MG3681A
Digital Modulation Signal Generator
Service Manual

Third Edition

To ensure that this equipment is used safely, important safety items are explained in the MG3681A Operation Manual. This document explains important service items related to service. Read both the operation manual and this document, and keep both with the MG3681A.

Measurement Solutions

ANRITSU CORPORATION

Document No.: M-W1708BE-3.0

Safety Symbols

To prevent the risk of personal injury or loss related to equipment malfunction, Anritsu Corporation uses the following safety symbols to indicate safety-related information. Insure that you clearly understand the meanings of the symbols BEFORE using the equipment.

Some or all of the following five symbols may not be used on all Anritsu equipment. In addition, there may be other labels attached to products which are not shown in the diagrams in this manual.

Symbols used in manual

DANGER 

This indicates a very dangerous procedure that could result in serious injury or death if not performed properly.

WARNING 

This indicates a hazardous procedure that could result in serious injury or death if not performed properly.

CAUTION 

This indicates a hazardous procedure or danger that could result in light-to-severe injury, or loss related to equipment malfunction, if proper precautions are not taken.

Safety Symbols Used on Equipment and in Manual

The following safety symbols are used inside or on the equipment near operation locations to provide information about safety items and operation precaution. Insure that you clearly understand the meanings of the symbols and take the necessary precautions BEFORE using the equipment.

This indicates a prohibited operation. The prohibited operation is indicated symbolically in or near the barred circle.

This indicates an obligatory safety precaution. The obligatory operation is indicated symbolically in or near the circle.

This indicates warning or caution. The contents are indicated symbolically in or near the triangle.

This indicates a note. The contents are described in the box.

These indicate that the marked part should be recycled.

MG3681A
Digital Modulation Signal Generator
Service Manual

25 April 2000 (First Edition)
10 April 2002 (Third Edition)

For Safety

For safety, do not open the equipment covers.

If repair is required, contact the sales representative, branch office, or agent at the telephone number and address given in this document or in the equipment operation manual.

Although not recommended by Anritsu Corporation, if it is really imperative to open the covers for emergency repair, take great care not to touch any dangerous parts.
Always request repair by a trained engineer who understands the hazards.

Anritsu Corporation will not accept liability for any injuries sustained as a result of opening the equipment covers.

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IBM and AT are registered trademark of International Business Machines Corporation.

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About This Manual

This Service Manual for the MG3681A Digital Modulation Signal Generator provides troubleshooting instructions on how to identify and replace faulty modules. Instructions on repairing the module's internal parts of a module are beyond the scope of this manual.

This service manual is written for our own and our dealers' service personnel who have completed a prescribed training course and are aware of fire, electrical shock and other accidents.

TABLE OF CONTENTS

SECTION 1
GENERAL

This service manual deals with the maintenance of the MG3681A Digital Modulation Signal Generator. It is organized into the following sections:

Section 1 General
Organization of this service manual

Section 2 Circuit Description
A description of the circuit operation of the signal generator and the functions of its component units, with reference to block diagrams

Section 3 Troubleshooting
Instructions on how to locate faults occurring in the signal generator

Section 4 Adjustment and Compensation
Instructions on how to adjust and compensate for the signal generator upon completion of troubleshooting

Section 5 Mechanical Configuration
Contains a list of parts to aid in troubleshooting and replacing faulty parts, plus removal instructions.

SECTION 2
CIRCUIT DESCRIPTION

2.1 Outline

This section describes the unit configuration of the MG3681A and introduces block diagrams for the individual units.

2.1.1 Outline of Circuitry

Table 2-1 gives a summary description of each component unit. Figure 2-1 shows a general block diagram.

Table 2-1 Outline of Circuitry

A No.	Name	Description
A01	MAIN MOTHER	• Feeds power and a control signal to the individual analog units. • Interfaces analog signals between the individual analog units. • Houses the rear-panel GPIB, RS-232C, Trigger, and PC Card connectors.
A02	DIGITAL MOTHER	• Feeds power and a control signal to the individual digital modulating units. • Interfaces baseband waveform data between the individual digital modulating units.
A03	REGULATOR	• Regulates DC voltages and removes noise. • Power switch control circuit.
A04	KEY ENCODE	• Generates key code data matched to key and rotary knob input. • Feeds power and drawing signals to the LCD. • Controls the step attenuator. • Controls the RPP (Reverse Power Protect) circuit. • Controls the audible alarm. • Selects between AC/DC coupling for external modulation signal input.
A05	REAR CONNECT	• Houses the digital input/output connector for the rear-panel digital modulating units. • Feeds power and a temperature control signal to the air-cooling fan.
A11	FRONT UNIT	• Contains the Front-Panel A1101 SWITCH BOARD, A1102 DISPLAY ASSEMBLY, and LCD Backlight Inverter.
A12	AUDIO / CLOCK	• Input buffer circuit for internally and externally supplied analog modulating signals. • Routes modulating signals according to the status of analog modulation using the switch matrix circuit. • Feeds the A23 LOCAL UNIT for FM or ϕM modulation. • Controls the modulating signal level according to the AM modulation depth setting and feeds it to the A22 I/Q MOD UNIT. • Generates a 4 kHz to 240 MHz clock signal used in the digital modulating units.
A1201	AF GENERATOR	• The DDS (Direct Digital Synthesizer) generates a 0.01 Hz to 400 kHz AF signal, with a resolution of 0.01 Hz, synchronized to a 100 MHz reference signal. • Feeds the AF signal for use in analog modulation. • Performs level and DC offset control on the AF signal and feeds the resultant signals for AF output. • The A1201 mounts in A12 as option 21.
A13	MAIN CPU	• Receives interrupts from sources, such as panel keys, triggers, and GPIB. • Generates and transmits hardware control data. • Generates display drawing data and transmits display signals. • Receives hardware status signals. • Backs up memory contents with a backup battery.
A16	POWER SUPPLY UNIT	• Generates a secondary power supply (+3.3 V, +5 V, ±7 V, ±13 V, +13 VS) from a primary power supply (100 to 120 VAC, 200 to 240 VAC). • Turns on or off all power output under power output control other than +13 VS. • Monitors the primary power status and generates a Power Fail signal.

Table 2-1 Outline of Circuitry (Continued)

A No.	Name	Description
A21	REFERENCE UNIT	• Houses a 10 MHz or 13 MHz reference crystal oscillator. • External reference signal input circuit • Provides a PLL circuit to generate a 100 MHz signal synchronized to a 10 MHz or 13 MHz reference signal. • Feeds the 100 MHz reference to the individual units. • Outputs a 10 MHz buffer signal.
A22	I/Q MOD UNIT	• Converts the baseband waveform data generated from the digital modulating units through to an internal I/Q signal (analog signal). • Removes the sampling clock noise superimposed by the internal I/Q signal through a smoothing filter. • Outputs the internal I/Q signal through the front panel. • Chooses between the internal and the external I/Q signal introduced from the front panel and feeds it in the vector modulator as a modulation signal. • Generates a 660 MHz IF and a 990 MHz/1650 MHz local signal synchronized with the 100 MHz reference signal with the synthesizer circuit. • Performs vector modulation on the 660 MHz IF signal with the I/Q signal and then pulse modulation with an FET switch-based pulse modulator. • Detects the IF signal emerging from vector and pulse modulation for use as an ALC circuit reference signal. • Superimposes the ALC reference signal on to the AM modulating wave generated from the A12 AUDIO/CLOCK to control the ALC reference signal level according to the output level setting. • Mixes the 660 MHz IF signal with a 990 MHz or 1650 MHz local signal according to the frequency setting, converts it to a 330 MHz, 660 MHz or 990 MHz IF signal, and then feeds it to the A24 3G RF UNIT.
A2202	EXT I/Q INTERFACE	• Performs a level change, DC offset, and polarity inversion on the I/Q output signal. • Mounts A2202 on to A2201 ASP as option 11.
A23	LOCAL UNIT	• Generates a 930 to 1590 MHz or 1670 to 3160 MHz local signal synchronized to the 100 MHz reference signal with a minimum resolution of 5 mHz; and then feeds the signal to the A24 3G RF UNIT. • Performs FM or ϕM modulation with the FM/ϕM modulating wave generated from the A12 AUDIO/CLOCK.
A24	3G RF UNIT	• Mixes the IF signal generated from the A22 I/Q MOD UNIT and the local signal generated from the A23 LOCAL UNIT together to generate a 0 to 3000 MHz RF output signal. • Passes the resultant mixed signal through a low-pass filter or band-pass filter matched to the output frequency to remove spurious signals. • Amplifies the signal with a power amplifier to get the final output level and feeds it to the step attenuator. • Detects the output signal level and returns it to the A22 I/Q MOD UNIT as an ALC comparison signal.
A26	POWER AMP UNIT	• Amplifies the output signal from A24 3G RF UNIT to output the higher-level signal. • A26 is to be installed when adding Option 42.

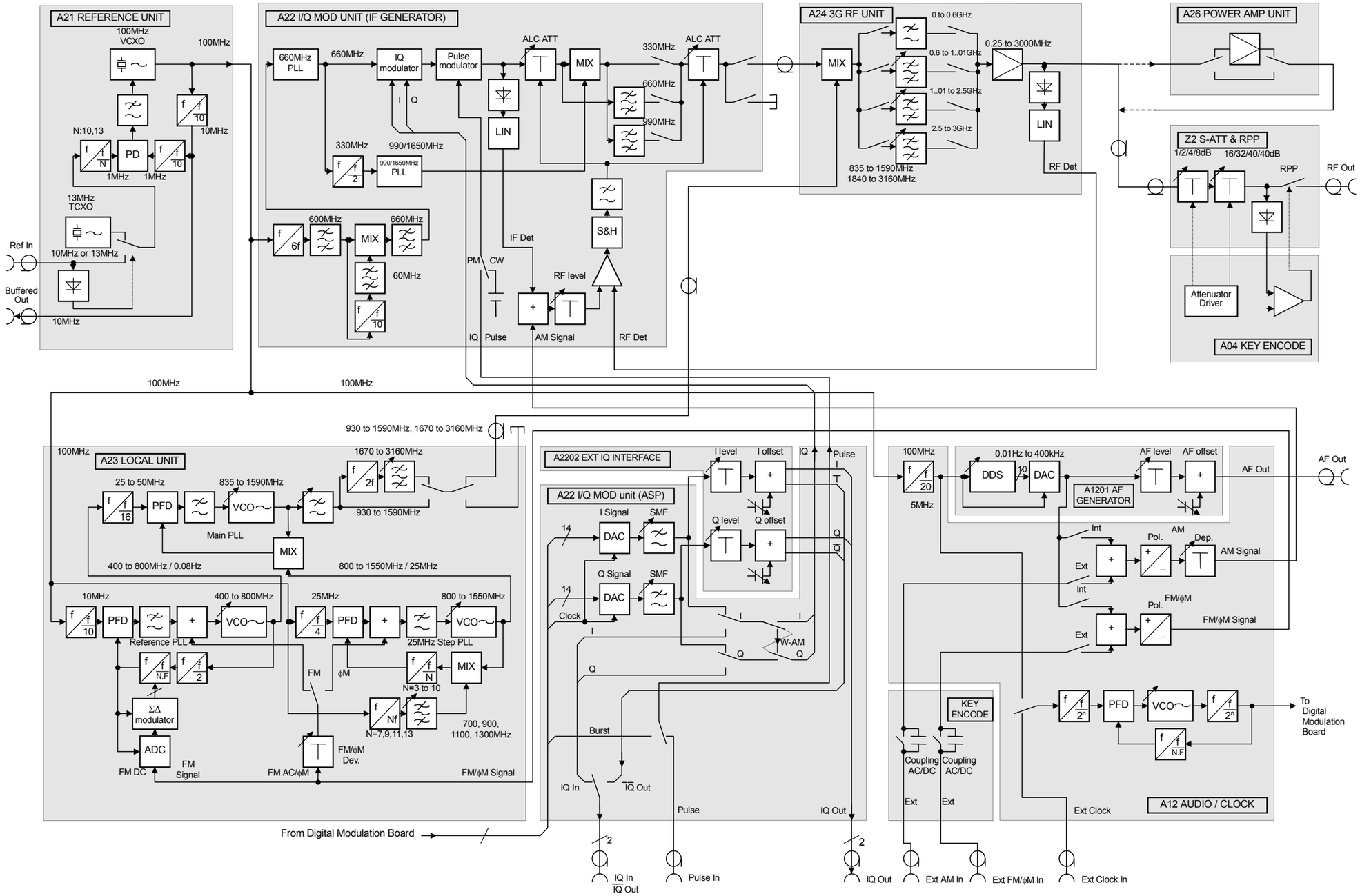


Fig.2-1 Overall Block Diagram

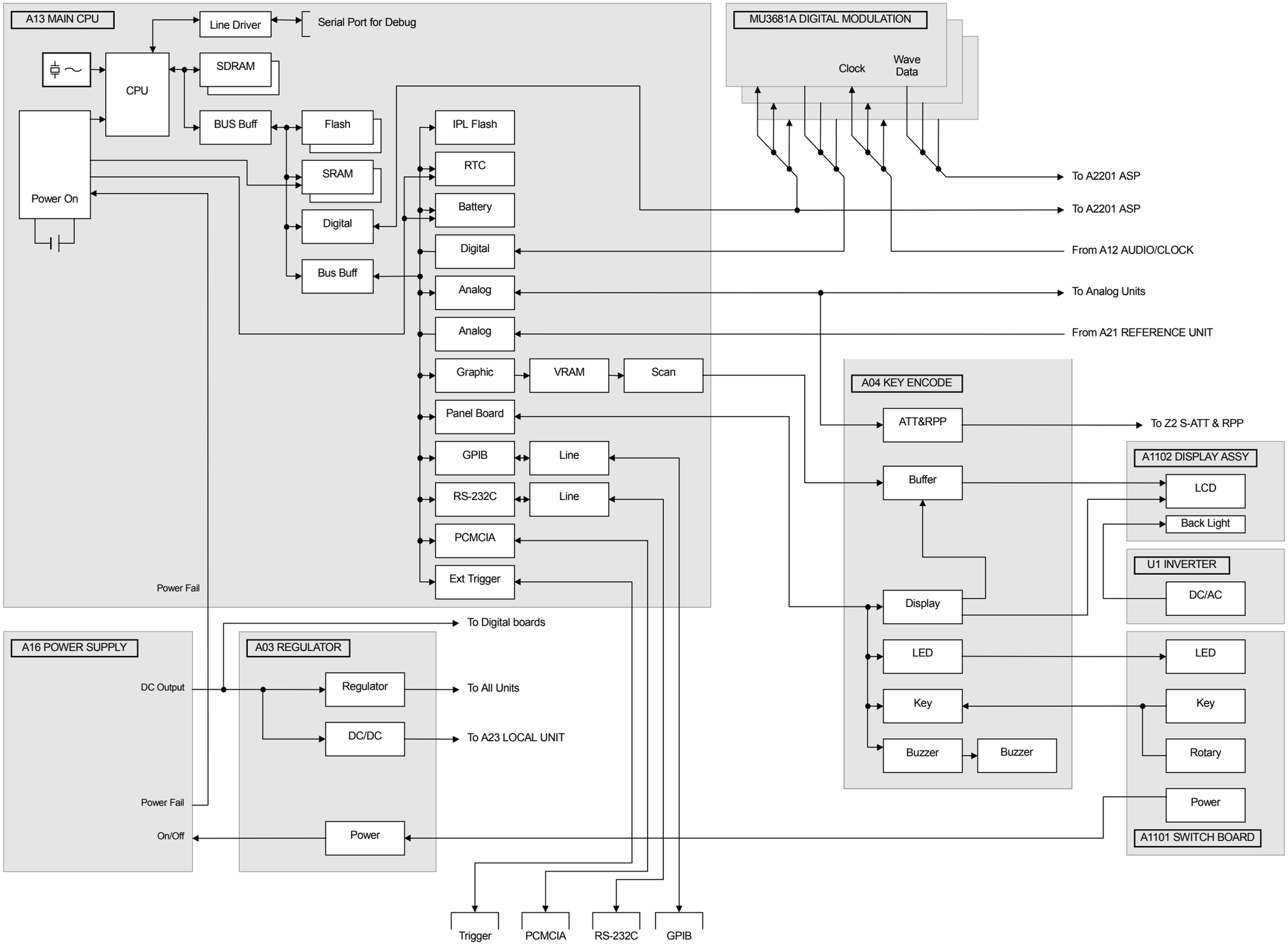


Fig.2-1 Overall Block Diagram (Continued)

2.1.2 Power Lines Description

The A16 POWER SUPPLY UNIT generates the seven secondary power supplies of +3.3 V, +5.0 V, ±7 V, ±13 V and standby +13 VS from the primary power supply.

The +3.3 V and +5 V supplies for digital circuitry are fed directly to the A12 AUDIO/CLOCK, the A13 MAIN CPU and digital modulating units via the A02 DIGITAL MOTHERBOARD.

After other power supplies are regulated and noise is removed by the A03 REGULATOR, they are fed to the individual units via the A01 MAIN MOTHERBOARD and the A02 DIGITAL MOTHERBOARD.

Table 2-2 lists the sources and voltages of the individual power lines. Figure 2-1 shows the power line flow in the MG3680 series.

Table 2-2 Power Lines

Output Power Lines	Power Source from A16	Functions at A03	Voltage Range
+3.3VD	+3.3V	Through	+3.3 to +3.7 V
+5.0VD	+5V	Through	+5.0 to +5.4 V
+6VA1	+7V	Regulator	+5.7 to +6.3 V
+6VA2			
+6VA3			
+6VA4			
+6VD1			
+6VD2			
-6VA1	-7V	Regulator	-5.7 to -6.3 V
-6VD1			
-6VD2			
+12VA1	+13V	Noise Filter	+12 to +16 V
+12VA2			
+12VD			
-12VA1	-13V	Noise Filter	-12 to -16 V
-12VA2			
-12VD			
+24V	+13V	DC-DC Converter	+22.8 to +25.2 V
+12VM	+13V	Regulator	+11.4 to +12.6 V
+12VS	+13VS	Regulator	+11.4 to +12.6 V
+5VE	+5V	Current Protector	+4.5 to +5.4 V

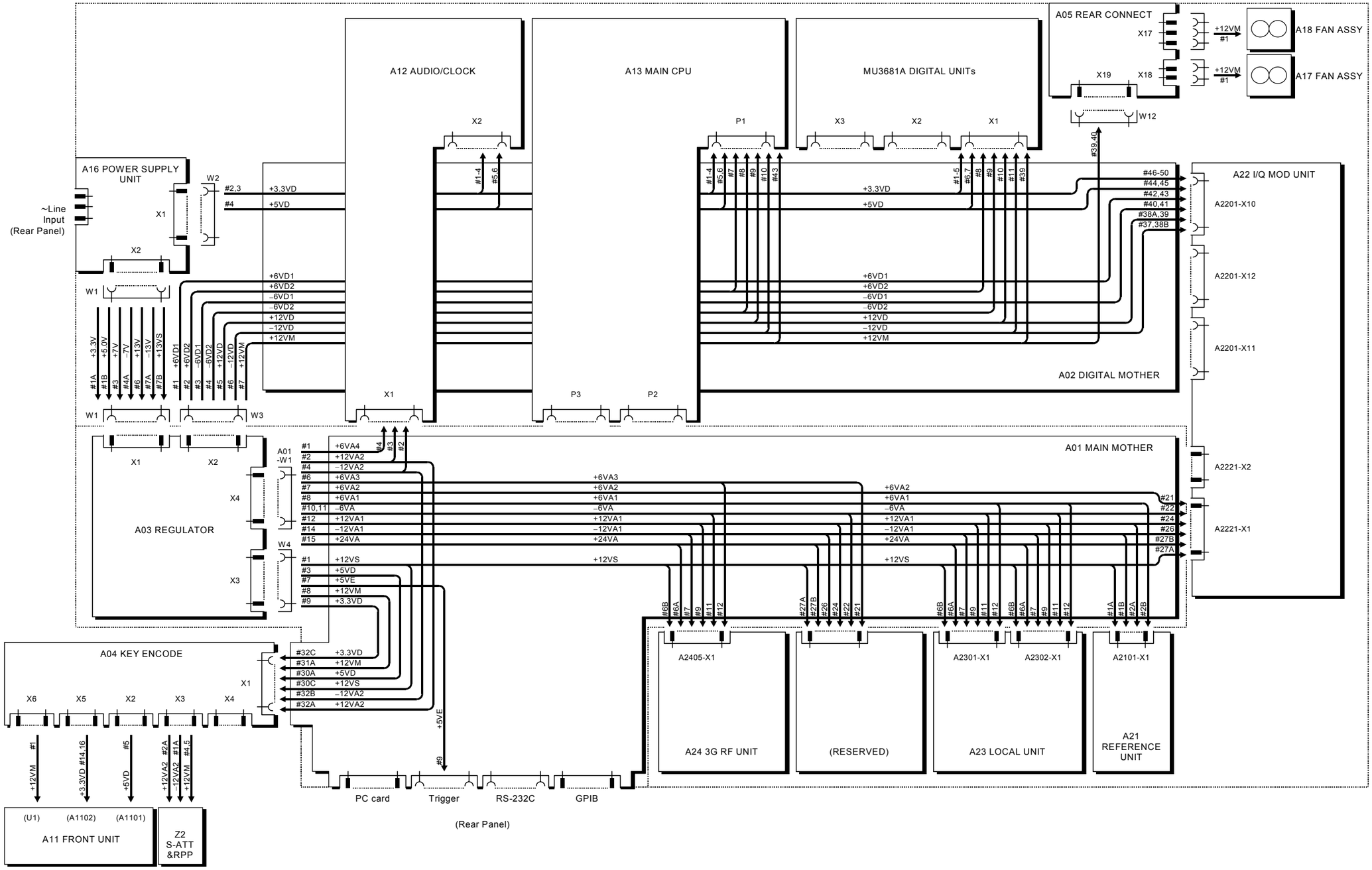


Fig.2-2 Power Line Diagram

2.1.3 Control Lines Description

The MG3681A hardware control is implemented by the A13 MAIN CPU. In internal digital modulation, the D/A converter mounted in the A22 I/Q MOD UNIT is controlled by the digital modulating units.
Table 2-3 gives a summary description of each of the main control lines. Figure 2-3 shows the control line flow in the MG3681A.

Table 2-3 Control Lines

Control Lines	Route	Remarks
Hardware control	ANALOG CONTROL BUS	Controls the individual analog units (A04, A12, A22, A23, A24) from A13.
	I/Q DATA BUS	Transfers internal digital modulating waveform data between the individual digital modulating units and the A2201 ASP.
	LCD SIGNAL	Feeds image drawing signals to the LCD display.
Status monitoring	PANEL BUS	Posts the status of key entry to A13 and controls on-panel LED lamps from A13.
	STATUS BUS	Posts the operating status of the individual analog hardware to A13.
Waveform data	DIGITAL CONTROL BUS	Controls the individual digital modulating units and the A2201 ASP from A13.
External interfaces	GPIB	GPIB external control
	RS-232C	RS-232C external control
	Trigger	Interrupt handling management by Trigger input
	PC card	PC card interface

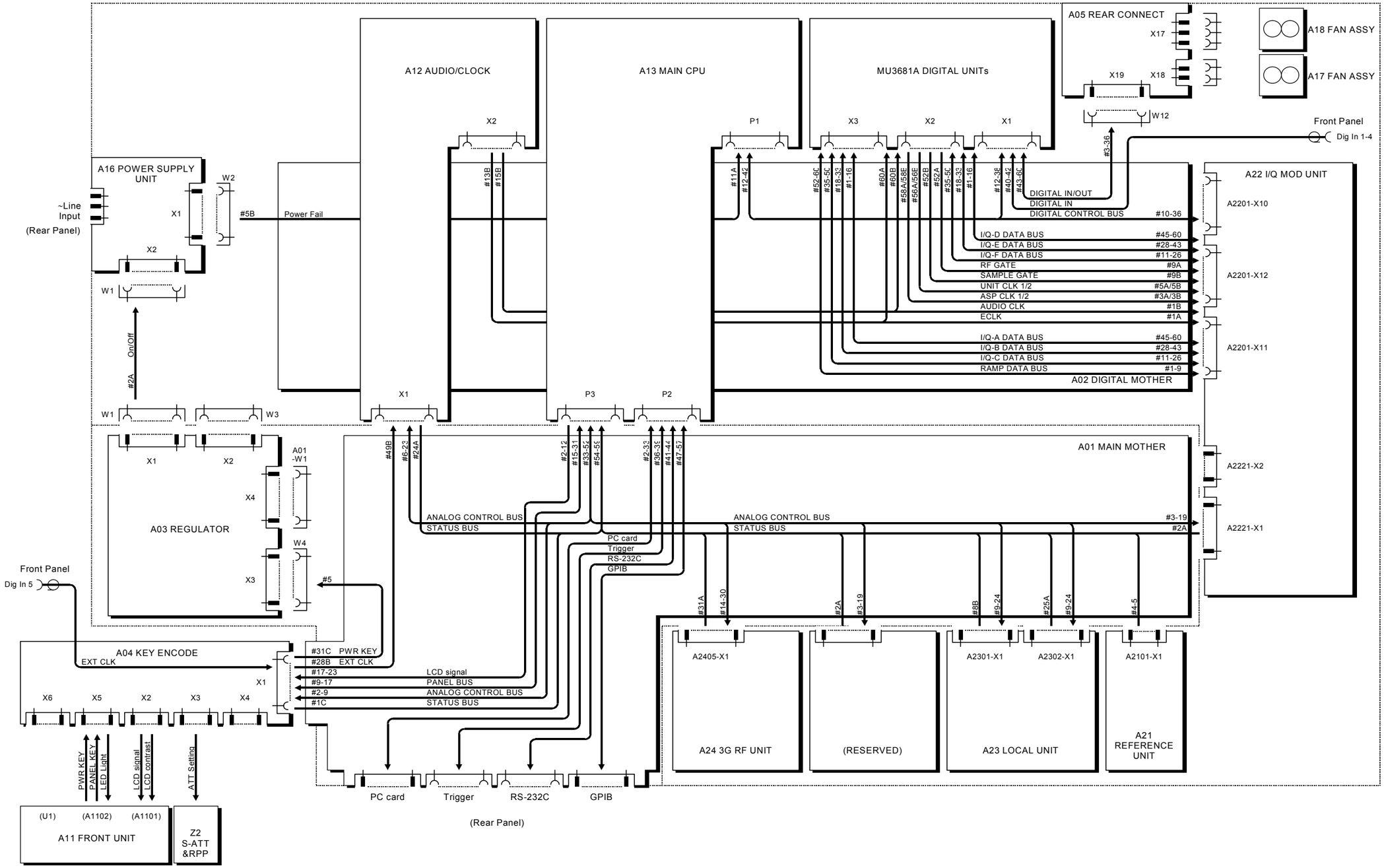


Fig.2-3 Control Line Diagram

2.1.4 Analog Lines Description

All analog circuits in the MG3681A frequency-convert the 100 MHz signal generated from the A21 REFERENCE UNIT to generate their final output signals.

The A22 I/Q MOD UNIT performs vector modulation (wide AM), pulse modulation or amplitude modulation to generate a 330, 660 or 990 MHz IF signal according to the output frequency.

The A23 LOCAL UNIT carries out frequency modulation or phase modulation to generate a 930 to 1590 MHz or 1670 to 3160 MHz local signal with a minimum resolution of 5 mHz, according to the output frequency.

The A24 3G RF UNIT beat up or down the IF signal generated from A22 I/Q MOD UNIT and the local signal generated from A23 LOCAL UNIT to convert them into a final output frequency signal.

Figure 2-4 shows the frequency relationships among the individual units. Figure 2-5 shows the flow of analog signals, their frequency and level relationships among the analog units.

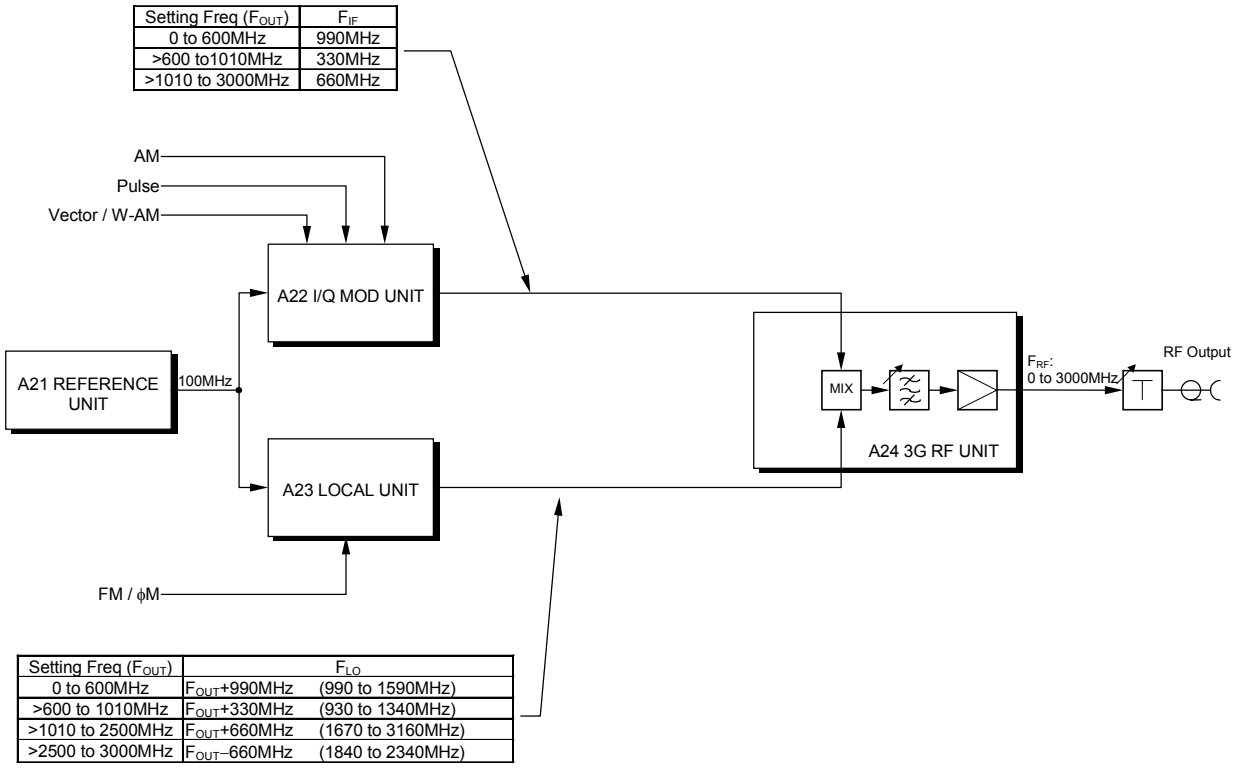


Fig.2-4 Frequency Diagram

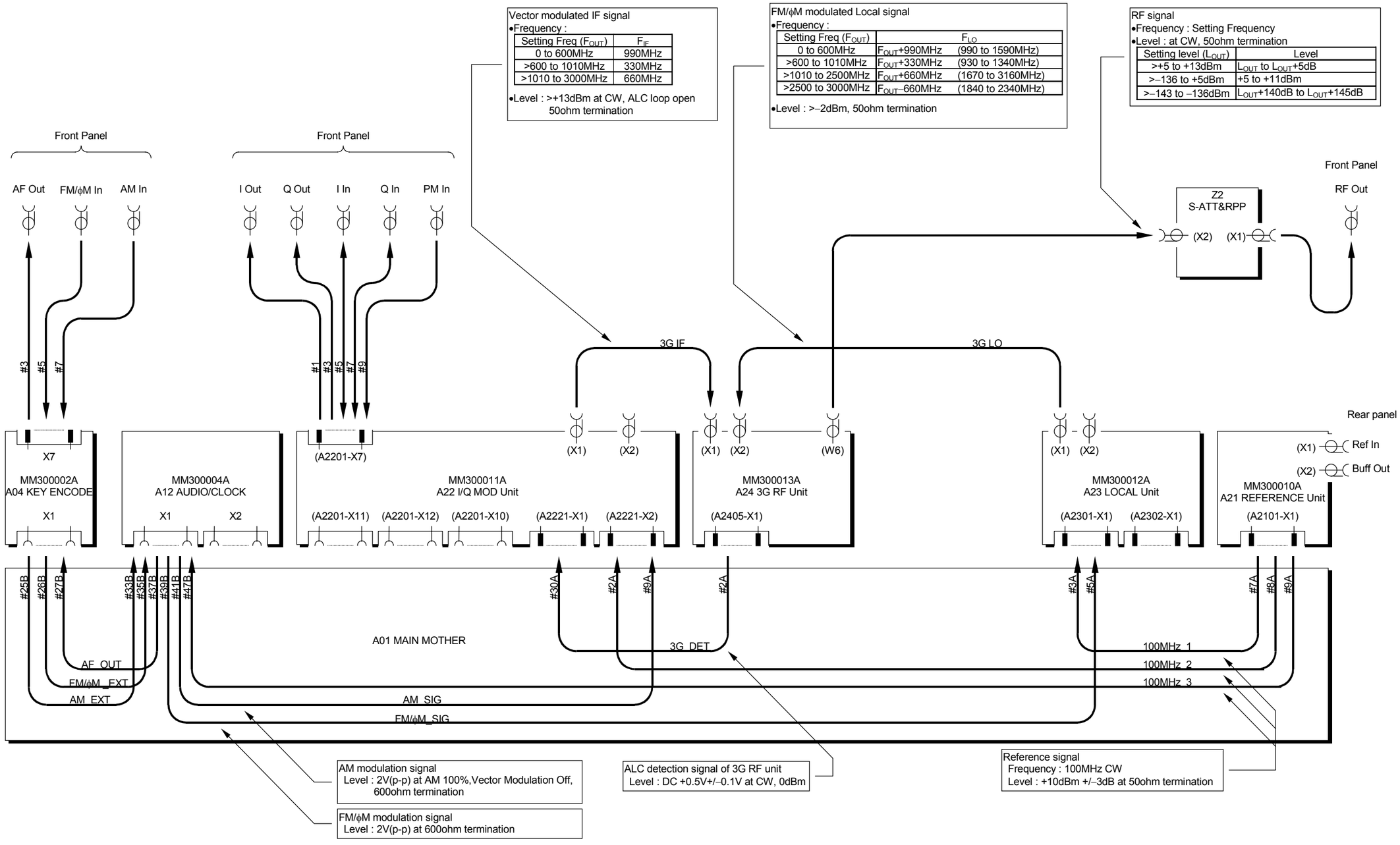


Fig.2-5 Analog Line Diagram

2.2 Circuit Description of Each Unit

2.2.1 A01 MAIN MOTHER

The A01 MAIN MOTHER, located under the chassis on the bottom of the equipment, accommodates the rear-panel GPIB, RS-232C, and trigger connectors. A PC card slot connector is also attached to the A01 MAIN MOTHER. All signal lines connected to the outside of the shielded case pass through a noise filter mounted on the PC board.
For signals passing though the A01 MAIN MOTHER, see Sections 2.1.2, 2.1.3 and 2.1.4.

2.2.2 A02 DIGITAL MOTHER

The A02 DIGITAL MOTHER is located above the chassis on the top of the equipment.
For signals passing though the A02 DIGITAL MOTHER, see Sections 2.1.2, 2.1.3 and 2.1.4.

2.2.3 A03 REGULATOR

The A03 REGULATOR is located under the chassis on the bottom of the equipment.
The A03 REGULATOR separates the five secondary power lines of ±7 V, ±13 V, and +13 VS from the A16 POWER SUPPLY UNIT into 19 lines according to their destination. It then regulates the voltages and removes noise before feeding the resultant voltages to the individual units via the A01 MAIN MOTHER and the A02 DIGITAL MOTHER. It also directs the two secondary power lines of +3.3 V and +5 V from the A16 POWER SUPPLY UNIT into the A01 MAIN MOTHER.
The A03 REGULATOR contains a power control circuit to enable the front-panel POWER key to control the output of the A16 POWER SUPPLY UNIT. The power control circuit consists of a flip-flop circuit to switch the output on and off with the POWER key signal and a latching relay to hold the on or off state.
Figure 2-6 shows a block diagram of the A03 REGULATOR.

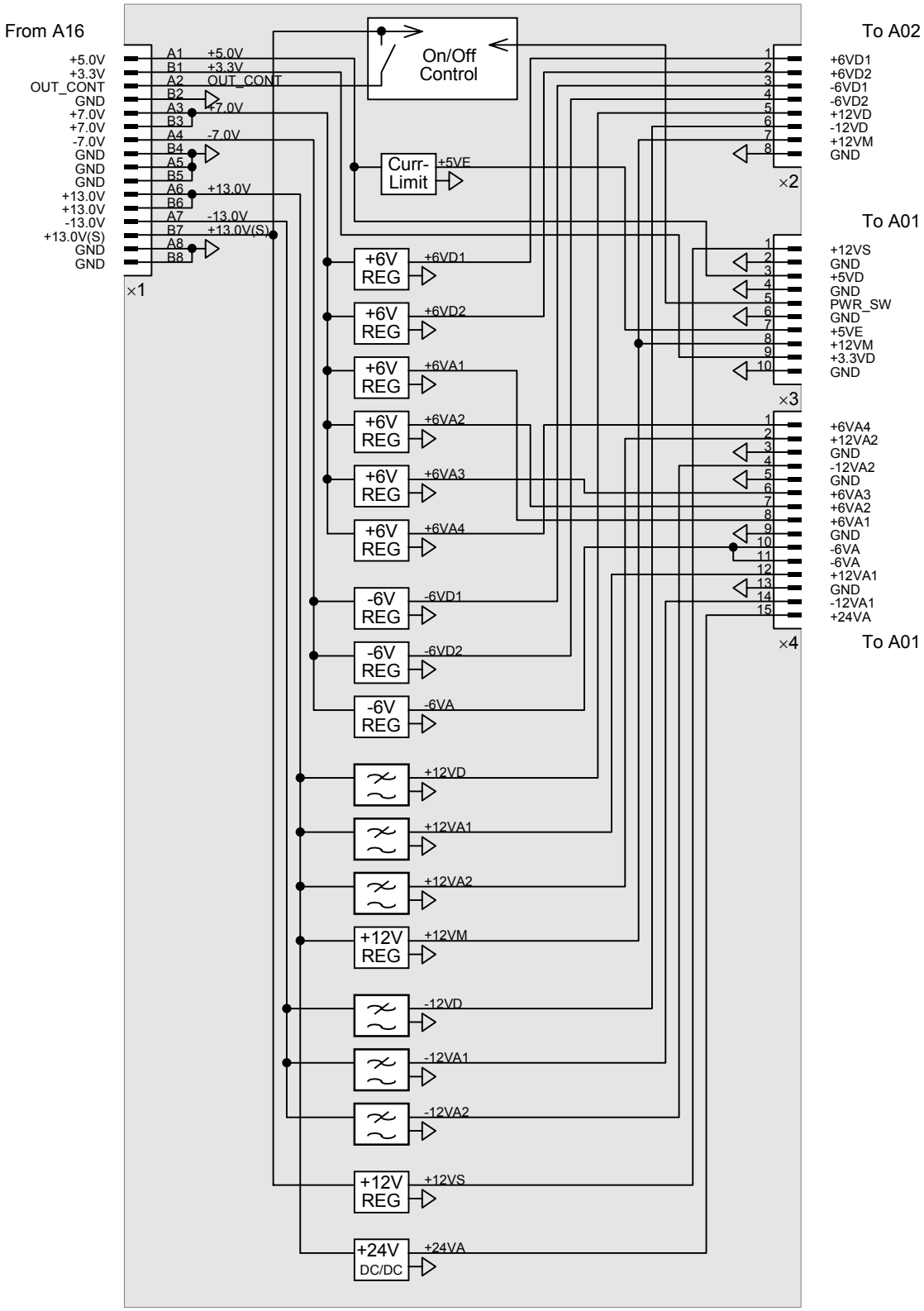


Fig.2-6 A03 REGULATOR Block Diagram

2.2.4 A04 KEY ENCODE

The A04 KEY ENCODE, located outside the shielded case on the front of the equipment, provides the following functions:

- Analyzes panel key and rotary encoder input signals and transmits key codes
  Analyzes the signals that are generated by operating the keys and the rotary knob on the A1101 SWITCH BOARD in the A11 FRONT UNIT, generates interrupts in the A13 MAIN CPU and transmits key codes.

- Turns on LED lamps
  Turns on the LED lamps on the A1101 SWITCH BOARD in the A11 FRONT UNIT according to set data from the A13 MAIN CPU.

- Feeds power and a control signal to the LCD display
  Feeds power to the A1102 DISPLAY ASSY in the A11 FRONT UNIT. This power supply has a switch circuit that is controlled by the Display On/Off function. Also relays the display signal generated by the A13 MAIN CPU. Contrast control is accomplished by feeding a contrast key signal from the A1101 SWITCH BOARD to an electronic potentiometer to control the contrast control voltage.

- Controls the audible alarm
  Sounds the audible alarm with a control signal from the A13 MAIN CPU. The duration of the audible alarm is controlled by a monostable multivibrator. The audible alarm is available in two durations for selective use: about 0.01 second for key click tones and about 1 second for error indications.

- Controls the step attenuator
  Drives a step attenuator that sets attenuations of 0 to 140 dB in steps of 1 dB according to the control signals from the A13 MAIN CPU. Table 2-4 lists the attenuations of the step attenuator associated with the output level setting.

- Controls the RPP (Reverse Power Protector)
  Compares the output voltage of the detector built in the step attenuator with a voltage equivalent of the cutoff power and, if the former is higher, sets the RS flip-flop circuit to turf off the cutoff switch built in the step attenuator.
  The RS flip-flop circuit is reset by a reset signal from the A13 MAIN CPU. Its operating status is transmitted to the A13 MAIN CPU as a status signal.

- Analog modulation external input circuit
  Terminates the signal from the front-panel AM Input and FM/ϕM Input connectors with a 600 Ω terminator to switch the AC/DC coupling. The input signal is fed to the A12 AUDIO/CLOCK.

- External clock input circuit
  Turns on or off the signal from the front-panel Digital Input 5 connector according to the usage status. The input signal is fed to the A12 AUDIO/CLOCK.

- Relays the power switch signal line
  Relays the power key signal from the A1101 SWITCH BOARD in the A11 FRONT UNIT to the A03 REGULATOR via the A01 MAIN MOTHER located in the shielded case.

Figure 2-7 shows a block diagram of the A04 KEY ENCODE.

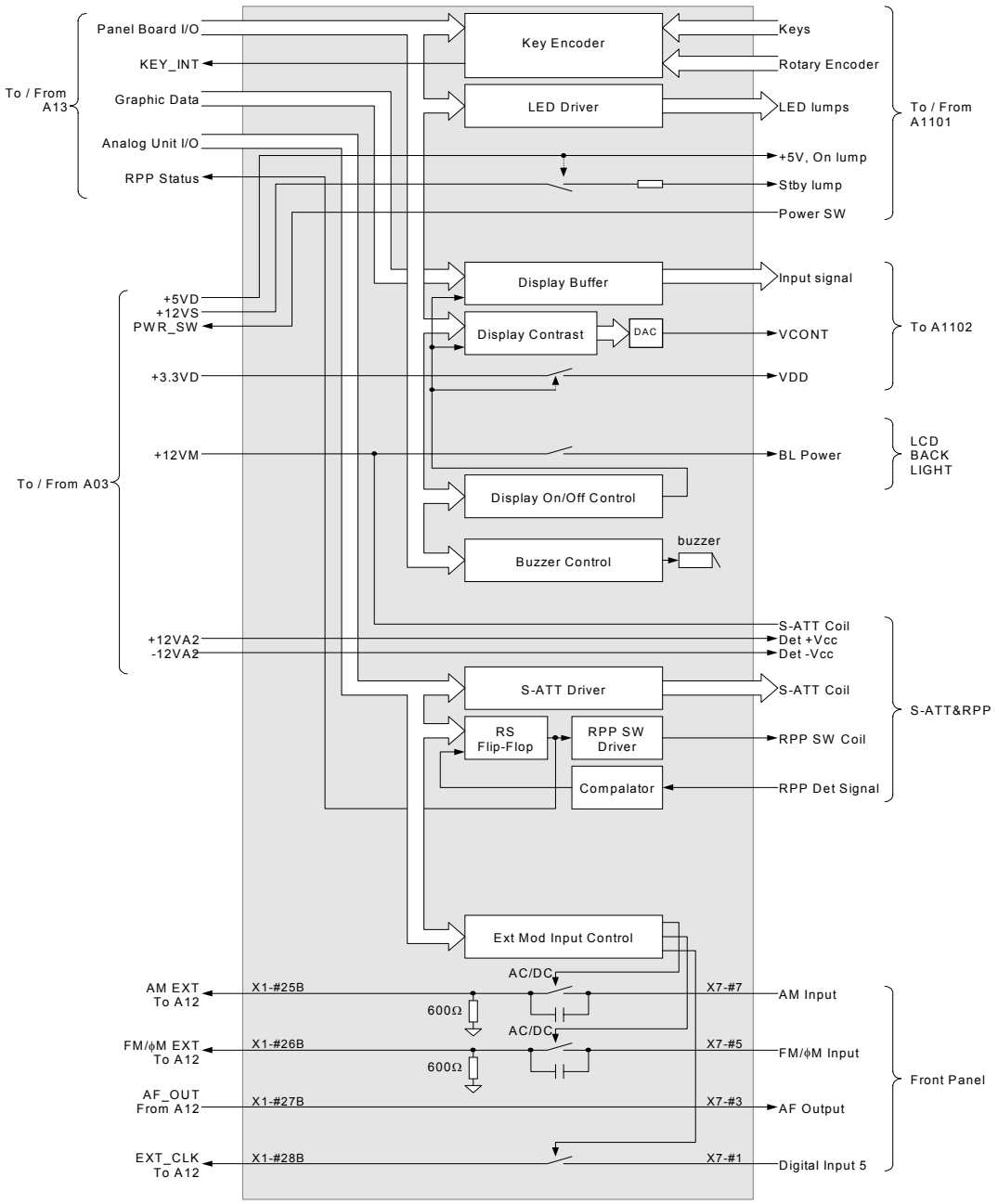
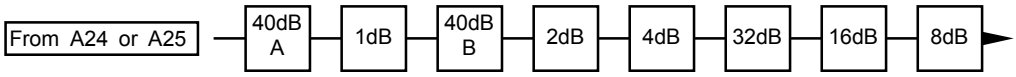


Fig.2-7 A04 KEY ENCODE Block Diagram

Table 2-4 Step Attenuator Setting



Output Level (at CW)	Total Attenuation	40dB-A	1dB	40dB-B	2dB	4dB	32dB	16dB	8dB
+17 to +4.01 dBm	0 dB		OFF		OFF	OFF			
+4 to +3.01 dBm	1 dB		ON		OFF	OFF			
+3 to +2.01 dBm	2 dB		OFF		ON	OFF			
+2 to +1.01 dBm	3 dB	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
+1 to +0.01 dBm	4 dB		OFF		OFF	ON			
0 to –0.99 dBm	5 dB		ON		OFF	ON			
–1 to –1.99 dBm	6 dB		OFF		ON	ON			
–2 to –2.99 dBm	7 dB		ON		ON	ON			
–3 to –3.99 dBm	8 dB		OFF		OFF	OFF			
: :	:	OFF	:	OFF	:	:	OFF	OFF	ON
–10 to –10.99 dBm	15 dB		ON		ON	ON			
–11 to –11.99 dBm	16 dB		OFF		OFF	OFF			
: :	:	OFF	:	OFF	:	:	OFF	ON	OFF
–18 to –18.99 dBm	23 dB		ON		ON	ON			
–19 to –19.99 dBm	24 dB		OFF		OFF	OFF			
: :	:	OFF	:	OFF	:	:	OFF	ON	ON
–26 to –26.99 dBm	31 dB		ON		ON	ON			
–27 to –27.99 dBm	32 dB		OFF		OFF	OFF			
: :	:	OFF	:	OFF	:	:	ON	OFF	OFF
–34 to –34.99 dBm	39 dB		ON		ON	ON			
–35 to –35.99 dBm	40 dB		OFF		OFF	OFF			
: :	:	OFF	:	OFF	:	:	ON	OFF	ON
–42 to –42.99 dBm	47 dB		ON		ON	ON			
–43 to –43.99 dBm	48 dB		OFF		OFF	OFF			
: :	:	OFF	:	OFF	:	:	ON	ON	OFF
–50 to –50.99 dBm	55 dB		ON		ON	ON			
–51 to –51.99 dBm	56 dB		OFF		OFF	OFF			
: :	:	OFF	:	OFF	:	:	ON	ON	ON
–58 to –58.99 dBm	63 dB		ON		ON	ON			
–59 to –59.99 dBm	64 dB		OFF		OFF	OFF			
: :	:	ON	:	OFF	:	:	OFF	ON	ON
–66 to –66.99 dBm	71 dB		ON		ON	ON			
–67 to –67.99 dBm	72 dB		OFF		OFF	OFF			
: :	:	ON	:	OFF	:	:	ON	OFF	OFF
–74 to –74.99 dBm	79 dB		ON		ON	ON			
–75 to –75.99 dBm	80 dB		OFF		OFF	OFF			
: :	:	ON	:	OFF	:	:	ON	OFF	ON
–82 to –82.99 dBm	87 dB		ON		ON	ON			
–83 to –83.99 dBm	88 dB		OFF		OFF	OFF			
: :	:	ON	:	OFF	:	:	ON	ON	OFF
–90 to –90.99 dBm	95 dB		ON		ON	ON			
–91 to –91.99 dBm	96 dB		OFF		OFF	OFF			
: :	:	ON	:	OFF	:	:	ON	ON	ON
–98 to –98.99 dBm	103 dB		ON		ON	ON			
–99 to –99.99 dBm	104 dB		OFF		OFF	OFF			
: :	:	ON	:	ON	:	:	OFF	ON	ON
–106 to –106.99 dBm	111 dB		ON		ON	ON			
–107 to –107.99 dBm	112 dB		OFF		OFF	OFF			
: :	:	ON	:	ON	:	:	ON	OFF	OFF
–114 to –114.99 dBm	119 dB		ON		ON	ON			
–115 to –115.99 dBm	120 dB		OFF		OFF	OFF			
: :	:	ON	:	ON	:	:	ON	OFF	ON
–122 to –122.99 dBm	127 dB		ON		ON	ON			
–123 to –123.99 dBm	128 dB		OFF		OFF	OFF			
: :	:	ON	:	ON	:	:	ON	ON	OFF
–130 to –130.99 dBm	135 dB		ON		ON	ON			
–131 to –131.99 dBm	136 dB		OFF		OFF	OFF			
–132 to –132.99 dBm	137 dB		ON		OFF	OFF			
–133 to –133.99 dBm	138 dB	ON	OFF	ON	ON	OFF	ON	ON	ON
–134 to –134.99 dBm	139 dB		ON		ON	OFF			
–135 to –143.00 dBm	140 dB		OFF		OFF	ON			

2.2.5 A05 REAR CONNECT

Located on the rear panel of the equipment, the A05 REAR CONNECT houses the rear-panel Digital Input/Output connector, which is connected to the digital modulating units via the A02 DIGITAL MOTHER.
Also feeds power and a temperature control signal to the rear-panel air-cooling fan. Temperature control of the air-cooling fan is regulated by a thermistor mounted on the A05 REAR CONNECT.

2.2.6 A11 FRONT UNIT

The A11 FRONT UNIT, mounted on the front panel of the equipment, includes the following units:

- A1101 SWITCH BOARD
  Consists of a key top rubber, a contact PC board, and a rotary encoder.
  The A1101 SWITCH BOARD is separated into two blocks with an intervening A1102 DISPLAY ASSY, and connected by a cable.

- A1102 DISPLAY ASSY
  The display surface of the D-STN LCD display is covered with a conductive gasket. The gasket is kept in contact with the shielding film attached to the acrylic plate of the display surface to suppress radio interference.

- U1 PH-BLC08-K2 INVERTER
  The PH-BLC08-K2 inverter is attached to the back of the A1102 DISPLAY ASSY, and its inverter output is wired to the backlight of A1102 DISPLAY ASSY.

The individual units mounted on the A11 FRONT UNIT are each wired to the A04 KEY ENCODE.

2.2.7 A12 AUDIO/CLOCK

The A12 AUDIO/CLOCK is inserted in the digital board shielded case on top of the equipment.
It generates an analog modulating signal and a clock signal for use in the digital modulating unit. When option 21 is installed, the A1201 AF GENERATOR is mounted onto the A12 AUDIO/CLOCK PC board.
The A12 AUDIO/CLOCK is made of the following functional blocks:

- Modulation matrix circuit
  Feeds the external modulating signal from the A04 KEY ENCODE and the internal modulating signal from the A1201 AF GENERATOR (option 21) to the AM modulating signal circuit and the FM/ϕM modulating signal circuit according to the modulation source setting.

- AM and FM/ϕM modulating signal polarity switching circuit
  Inverts or non-inverts the AM and FM/ϕM modulating signals selected by the modulation matrix circuit.

- AM modulation factor setting circuit
  Provides a 12-bit multiplier DA converter to vary the AM modulation factor between 0 and 100% with an equivalent resolution of 0.1%.

- AM modulating signal output circuit
  Outputs an AM modulating signal to the A22 I/Q MOD UNIT with an output impedance of 600 Ω and an output level of 2 Vp-p (terminated by 600 Ω with 100% AM and vector modulation is off).

- FM/ϕM modulating signal output circuit
  Outputs an FM/ϕM modulating signal to the A23 LOCAL UNIT with an output impedance of 1 kΩ and an output level of 2 Vp-p (terminated by 1 kΩ).

- Internal modulating signal generating AF output circuit (A1201 AF GENERATOR)
  The Direct Digital Synthesizer (DDS) generates a 0.01 Hz to 400 kHz AF signal, with a resolution of 0.01 Hz, synchronized to the 100 MHz reference signal generated from the A21 REFERENCE UNIT.
  The AF signal thus generated is fed to the A12 AUDIO/CLOCK for use in analog modulation. A 12-bit multiplier DA converter varies the AF level between 0 and 4 Vp-p with an equivalent resolution of 1 mVp-p, adding a 1 mV equivalent of DC voltage with a DC offset of -2 to +2 V to output from the front-panel AF Output connector via the A12 AUDIO/CLOCK.

- Internal synchronization clock generation circuit
  Generates a 4 kHz to 240 MHz clock signal, with a resolution of 1 Hz, synchronized to the 100 MHz internal reference signal supplied from the A21 REFERENCE UNIT and feeds it to the individual digital modulating boards.

- External synchronization clock generation circuit
  As the external clock signal is supplied the front-panel Digital Input 5 connector, it is fed to the synthesizer circuit as a reference signal via the a TTL level (10 kHz to 32 MHz, DC coupled) or 0.5 Vp-p, 50 Ω (1 MHz to 32 MHz, AC coupled) input circuit, according to the setting. The synthesizer generates a two, four, eight, or 16 times higher frequency clock signal synchronized with the input clock signal and feeds it to the digital modulating boards.

- PLL error detection circuit
  Generates a status signal in the A13 MAIN CPU by assuming a clock generation synthesizer error in any of the following situations:
  - The PLL is unlocked due to a hardware fault.
  - External clock input is interrupted during external input signal synchronization clock output.
  - Clock input of 0.5 Vp-p, 50 Ω is supplied over an external input signal interface set at the TTL level.

Figure 2-8 shows a block diagram of the A12 AUDIO/CLOCK and the A1201 AF GENERATOR.

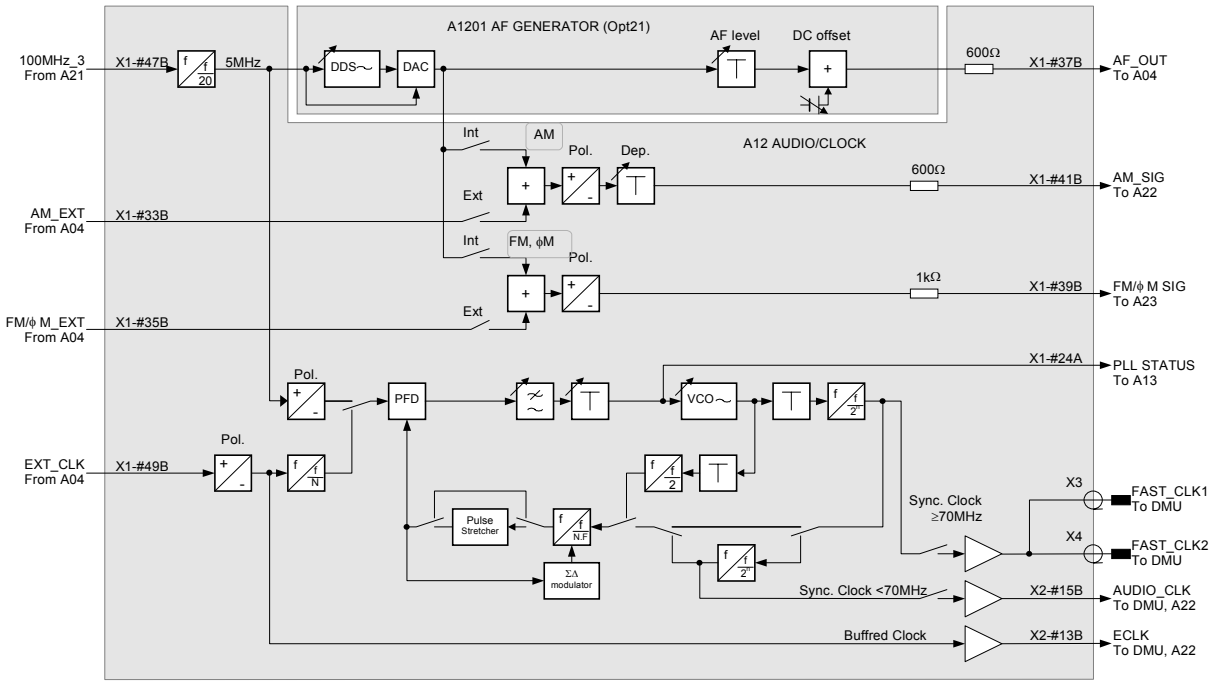


Fig.2-8 A12 AUDIO/CLOCK and A1201 AF GENERATOR Block Diagram

2.2.8 A13 MAIN CPU

The A13 MAIN CPU is inserted in the digital board shielded case on top of the equipment. It is a control circuit that controls functionality of this equipment and all the units. It includes the following functional blocks:

- CPU
  The HD6417708SF60-based CPU has a crystal oscillator, a reset IC and other peripheral circuits.

- IPL memory
  Composed of flash memory, the IPL memory stores a program that is launched when the equipment is turned on.

- Flash memory
  Flash memory is used in a memory that stores a program that implements the functionality of the equipment. Memory contents can be rewritten by downloading from the PC card.

- SDRAM
  Work memory to store setup parameters, etc. when the equipment runs.

- SRAM
  Backup memory that backs up setup parameters needed in times of power failures. Stored data is backed up by a lithium battery.

- Real-time clock
  Calculates the current date and time. The real-time clock is constantly run by a lithium battery. The date and time are set by an external controller via GPIB.

- Lithium battery
  Mounted to back up SRAM data and run the real-time clock.

- Graphics controller
  The ARTOP-based graphics controller has drawing data drawn by ARTOP in multiport VRAM.

- Scan controller
  Converts drawing data output from multiport VRAM to a timing signal matched to the LCD.

- LCD controller
  Turns on or off the LCD backlight and the LCD power, and also generates drawing data and synchronization signal to display LCD images.

- Digital unit bus
  An interface that controls the digital modulating units.

- Analog unit bus
  An interface that controls the analog units.

- Analog unit status
  Reads flags that represent the operating status of the analog units.

- Keyboard bus
  Carries out communication with the panel keys, generating interrupts from key entry as its basic operation. These interrupts enable the CPU to read keyboard data and determine which key has been pressed.

- GPIB interface
  The GPIB control interface is made up of a GPIB interface IC and a line driver. The GPIB connector is mounted on the A01 MAIN MOTHER.

- RS-232C interface
  The RS-232C control interface is made up of an RS-232C interface IC and a line driver. The RS-232C connector is mounted on the A01 MAIN MOTHER.

· PC card interface
A PCMCIA-compliant flash memory card-ready interface consists of a power IC and a card controller. The PC card slot is mounted on the A01 MAIN MOTHER.

Figure 2-9 shows a block diagram of the A13 MAIN CPU.

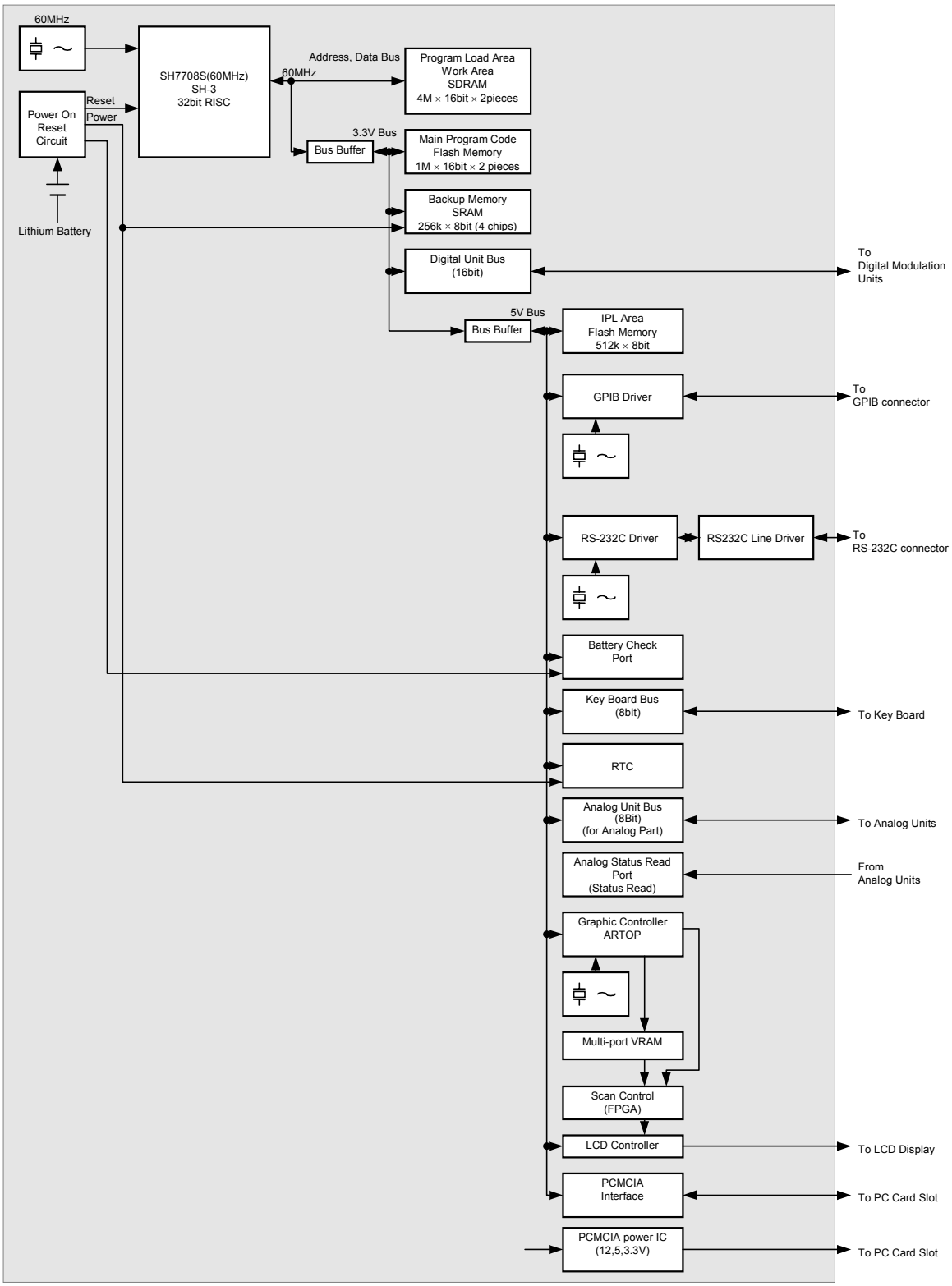


Fig.2-9 A13 MAIN CPU Block Diagram

2.2.9 A16 POWER SUPPLY UNIT

The A16 POWER SUPPLY UNIT is an integral part of the rear-panel power inlet and power switch. It is mounted on top of the equipment.

The A16 POWER SUPPLY UNIT converts a primary power supply (100 to 120 VAC, 200 to 240 VAC) into the seven secondary power supplies of +3.3 V, +5.0 V, ±7 V, and ±13 V and standby +13 VS. It also turns on or off power output under power output control, other than +13 VS. This is controlled by using a signal converted to an ON/OFF signal by the A03 REGULATOR representing the front-panel POWER key operation.

The A16 POWER SUPPLY UNIT monitors the status of the primary power supply and reports faults, such as momentary interruptions, to the A13 MAIN CPU.

All power output is protected from shorts and overloads by an overcurrent protection circuit. When the overcurrent protection circuit trips, all power output stops. The protective circuit will also trip in the event of abnormal temperature increases in the units. The protective circuit is reset by turning on the primary power supply.

2.2.10 A21 REFERENCE UNIT

The A21 REFERENCE UNIT is mounted on to of the rear panel. It generates a 100 MHz signal synchronized to the 13 MHz or 10 MHz oscillator signal that serves as a reference clock and then transmits it to the A12 AUDIO/CLOCK, the A22 I/Q MOD UNIT and the A23 LOCAL UNIT.

When a 10 MHz or 13 MHz reference signal is fed from the rear-panel Reference Input connector, the A21 REFERENCE UNIT synchronizes the 100 MHz signal to that signal as a reference clock.

The A21 REFERENCE UNIT is built from three PC boards. The A2101 100 MHZ PLL is a PLL circuit that is assembled of a 100 MHz VCXO, a frequency divider, a PFD and a loop filter. The 100 MHz signal generated is fed to the A12 AUDIO/CLOCK, the A22 I/Q MOD UNIT and the A23 LOCAL UNIT via the A01 MAIN MOTHER.

The A2102 STD SWITCH detects the reference signal from the rear-panel Reference Input connector and switches to the external signal or internal reference oscillator, dividing the signal by 10 or 13 to produce 1 MHz for transmission to the A2101 100 MHZ PLL.

The A2103 STD OSC holds a 13 MHz TCXO to produce an internal reference signal. Replace this PC board with A2104 or A2105 in case of mounting either the option 01 or 02 reference crystal oscillator. Table 2-5 lists the crystal oscillators that are used to produce reference clocks.

The A2102 STD SWITCH and the A2103 STD OSC can be removed from the rear panel together with the Reference Input connector and the Buffer Output connector, without removing the A21 REFERENCE UNIT.

Figure 2-10 shows a block diagram of the A21 REFERENCE UNIT.

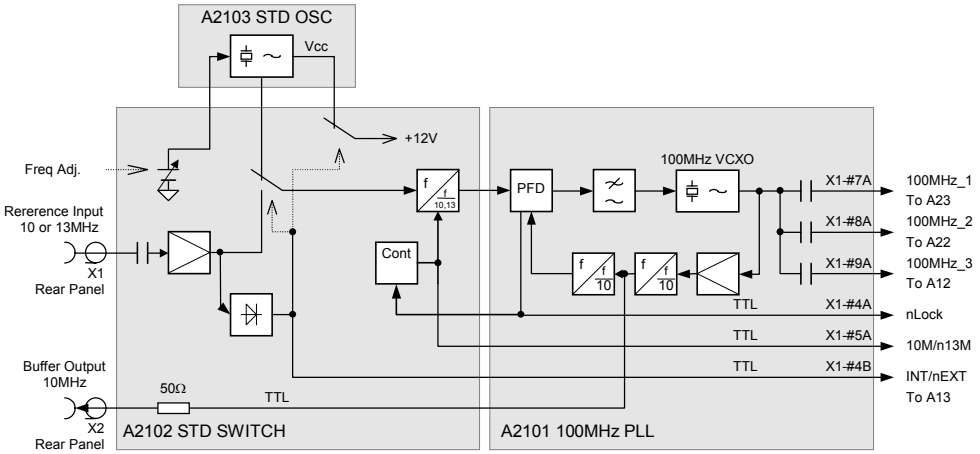


Fig.2-10 A21 REFERENCE UNIT Block Diagram

Table 2-5 Crystal Oscillators

	PC board	Frequency	Aging Rate	Temperature stability (0 to 50°C)	Notes
Standard	A2103	13 MHz	$\pm 1 \times 10^{-6}$/year	$\pm 1 \times 10^{-6}$	TCO-987A2-13MHz
Option 01	A2104	10 MHz	$\pm 5 \times 10^{-9}$/day	$\pm 3 \times 10^{-8}$	TCO-672A
Option 02	A2105	10 MHz	$\pm 5 \times 10^{-10}$/day	$\pm 5 \times 10^{-9}$	TCO-672B

2.2.11 A22 I/Q MOD UNIT

The A22 I/Q MOD UNIT, housed in an aluminum-shielded casing, is inserted in the top of the equipment. The A22 I/Q MOD UNIT is made up of two PC boards: the A2201 ASP, which generates a digital modulating baseband signal, and the A2221 IF GENERATOR, which generates an IF signal for vector modulation. When Option 11 is available, the A2202 EXT I/Q INTERFACE is mounted on the A2201 ASP PC board.
The A2201 ASP is made up of the following functional blocks:

- D/A converter
  Converts the baseband waveform data generated from the digital modulating units to an internal I/Q signal (analog signal).

- Smoothing filter
  Removes the sampling clock noise contained in the internal I/Q signal. This signal is fed to the vector modulator in the A2221 IF GENERATOR as an internal modulating signal.

- I/Q signal output circuit
  Generates the I/Q signal that emerges from the smoothing filter of the front-panel I/Q Output connector with an output impedance of 50 Ω.
  When Option 11 is available, the I/Q signal is generated via the A2202 EXT I/Q INTERFACE. This interface generates an I/Q signal which is an inverted signal $\overline{I}/\overline{Q}$ and sets the level, DC offset and orthogonality.

- External I/Q signal input circuit
  Feeds the I/Q signal received from the front-panel I/Q Input connector to the vector modulator in the A2221 IF GENERATOR when external digital modulation is selected. The I/Q Input connector signal line is terminated by 50 Ω.

- I/Q signal sampling circuit (A2203 I/Q SAMPLING)
  Samples the I/Q signal with an A/D converter and transmits it to the A13 MAIN CPU for use in crest ratio display.

The A2221 IF GENERATOR is made up of the following functional blocks:

- IF signal generation circuit
  Generates a 660 MHz IF signal synchronized with the 100 MHz reference signal; also generates 990 MHz/1650 MHz local signals from a synthesizer circuit to convert the IF signal to 330 MHz and 990 MHz, and then feeds them to the IF frequency conversion circuit.

- Vector modulator
  Performs vector modulation on the 660 MHz IF signal with the I/Q modulating signal fed from the A2201 ASP. As the spectrum of the IF signal is inverted depending on the frequency setting, the I/Q signal is replaced by the A2201 ASP to have the spectrum of the IF signal inverted beforehand.

- Pulse modulator
  Performs pulse modulation on the IF signal resulting from vector modulation with a FET switch. In pulse modulation, the modulating signal is fed from the front-panel Pulse Input connector via the A2201 ASP; in burst modulation, a burst trigger signal generated from the digital modulating units is fed via the A2201 ASP.

- ALC circuit
  Detects the IF signal resulting from vector and pulse modulation to provide a reference signal to the ALC circuit. The ALC reference signal is superimposed with the AM modulating wave generated from the A12 AUDIO/CLOCK and its voltage is varied between -8 and +17 dBm with an equivalent resolution of 0.01 dB in a mix of a 12-bit multiplier D/A converter and a 1/4 attenuator.
  The voltage of this ALC reference signal and that of the final output detection signal from the A24 3G RF UNIT are compared and the variable attenuator in the IF signal route is controlled to make the two voltages equal so as to set and stabilize the final level.

· IF frequency conversion circuit
  Mixes the 660 MHz IF signal with a 990 or 1650 MHz local signal according to the frequency setting to convert to a 330, 660 or 990 MHz IF signal, which is fed to the A24 3G RF UNIT.

Table 2-6 summarizes the relationships between the output frequency of this equipment and the IF frequency of the A22 I/Q MOD UNIT.
Figures 2-11 and 2-12 show block diagrams of the A22 I/Q MOD UNIT.

Table 2-6 Output frequency vs. IF frequency

Output frequency (F_{OUT})	IF frequency (F_{IF})	IF signal polarity
0 to 600 MHz	990 MHz (1650M - 660M)	Positive
>600 to 1010 MHz	330 MHz (990M - 660M)	Positive
>1010 to 2500 MHz	660 MHz	Positive
>2500 to 3000 MHz	660 MHz	Negative

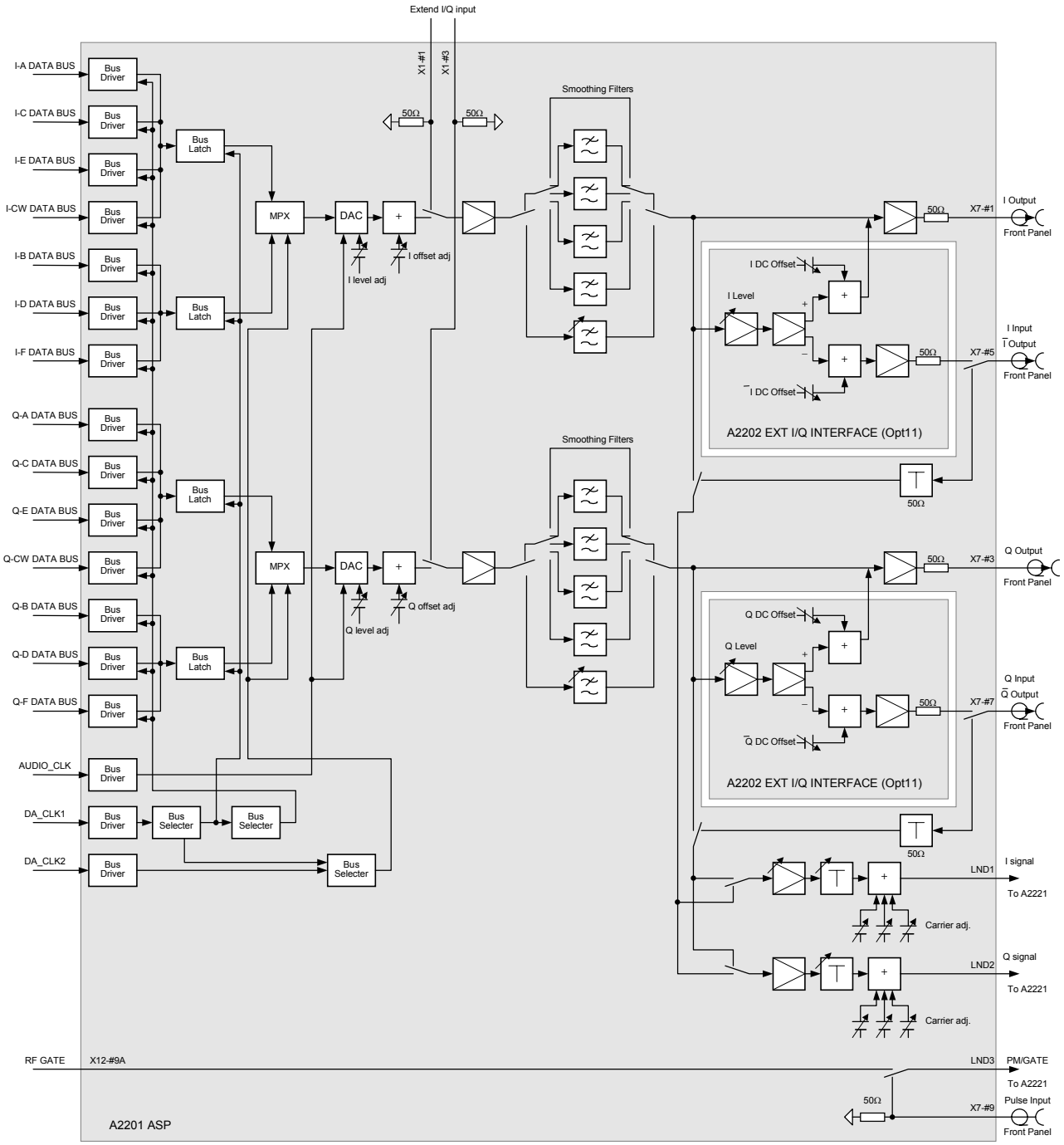


Fig.2-11 A22 I/Q MOD UNIT (A2201 ASP) Block Diagram

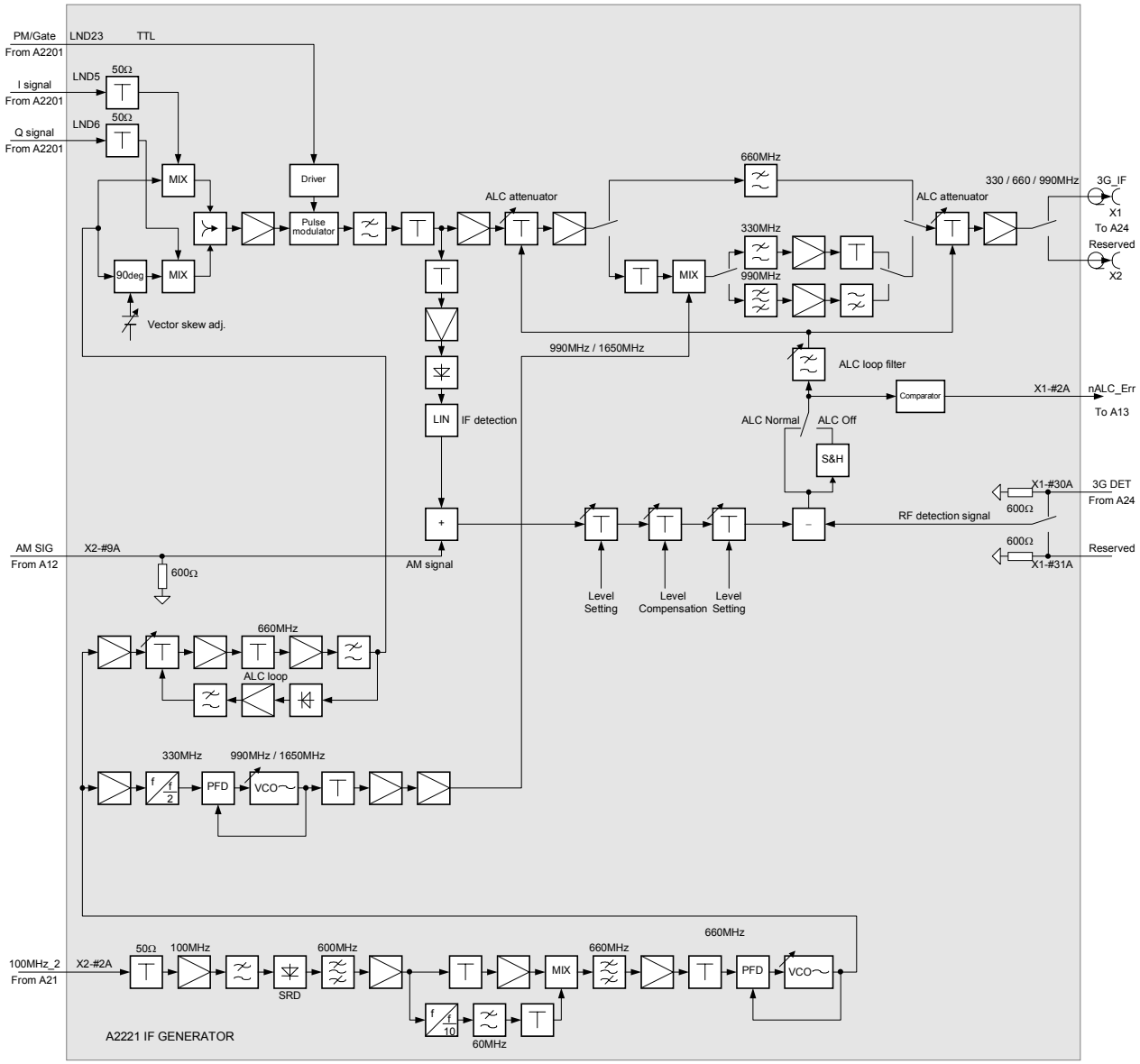


Fig.2-12 A22 I/Q MOD UNIT (A2221 IF GENERATOR) Block Diagram

2.2.12 A23 LOCAL UNIT

The A23 LOCAL UNIT, structured in an aluminum-shielded case, is inserted in the top of the equipment. It generates a 930 to 1590 MHz or 1670 to 3160 MHz local signal, with a minimum resolution of 5 mHz, synchronized to the 100 MHz reference signal fed from the A21 REFERENCE UNIT.

The A23 LOCAL UNIT also performs FM and ϕM with the FM/ϕM modulating signal fed from the A12 AUDIO/CLOCK.

Table 2-7 summarizes the relationships between the output frequency of this equipment and local frequency of the A23 LOCAL UNIT.

Table 2-7 Output frequency vs. Local frequency

Output frequency (F_{OUT})	Local frequency (F_{LOCAL})
0 to 600 MHz	F_{OUT} + 990 MHz (990 to 1590 MHz)
>600 to 1010 MHz	F_{OUT} + 330 MHz (930 to 1340 MHz)
>1010 to 2500 MHz	F_{OUT} + 660 MHz (1670 to 3160 MHz)
>2500 to 3000 MHz	F_{OUT} − 660 MHz (1840 to 2340 MHz)

The A23 LOCAL UNIT comprises three PC boards.

A2301 LOCAL 1 is built using a 25 MHz step PLL, which generates an 800 to 1550 MHz with a 25 MHz resolution, and a Reference PLL, which generates a 400 to 800 MHz with a 0.04 Hz resolution. ϕM is a 25 MHz step PLL. FM is modulated by the Reference PLL.

The Main PLL for A2302 LOCAL 2 generates an 835 to 1590 MHz, 0.0025 Hz resolution signal by adding the 25 to 50 MHz, 0.0025 Hz resolution signal which was divided by 16 and the signal from the 25 MHz Step PLL to the signal from the Reference PLL which was generated by the A2301 LOCAL 1.

The A2303 DOUBLER chooses between the signal as generated from A2302 LOCAL 2 and the signal with a two-time higher frequency to generate a 930 to 1590 MHz signal with a 0.0025 Hz resolution or a 1670 to 3160 MHz signal with a 0.005 Hz resolution.

Figure 2-13 shows the relationships between the 25 MHz step PLL and Reference PLL frequencies and the local frequency. Figure 2-14 shows a block diagram of the A23 LOCAL UNIT.

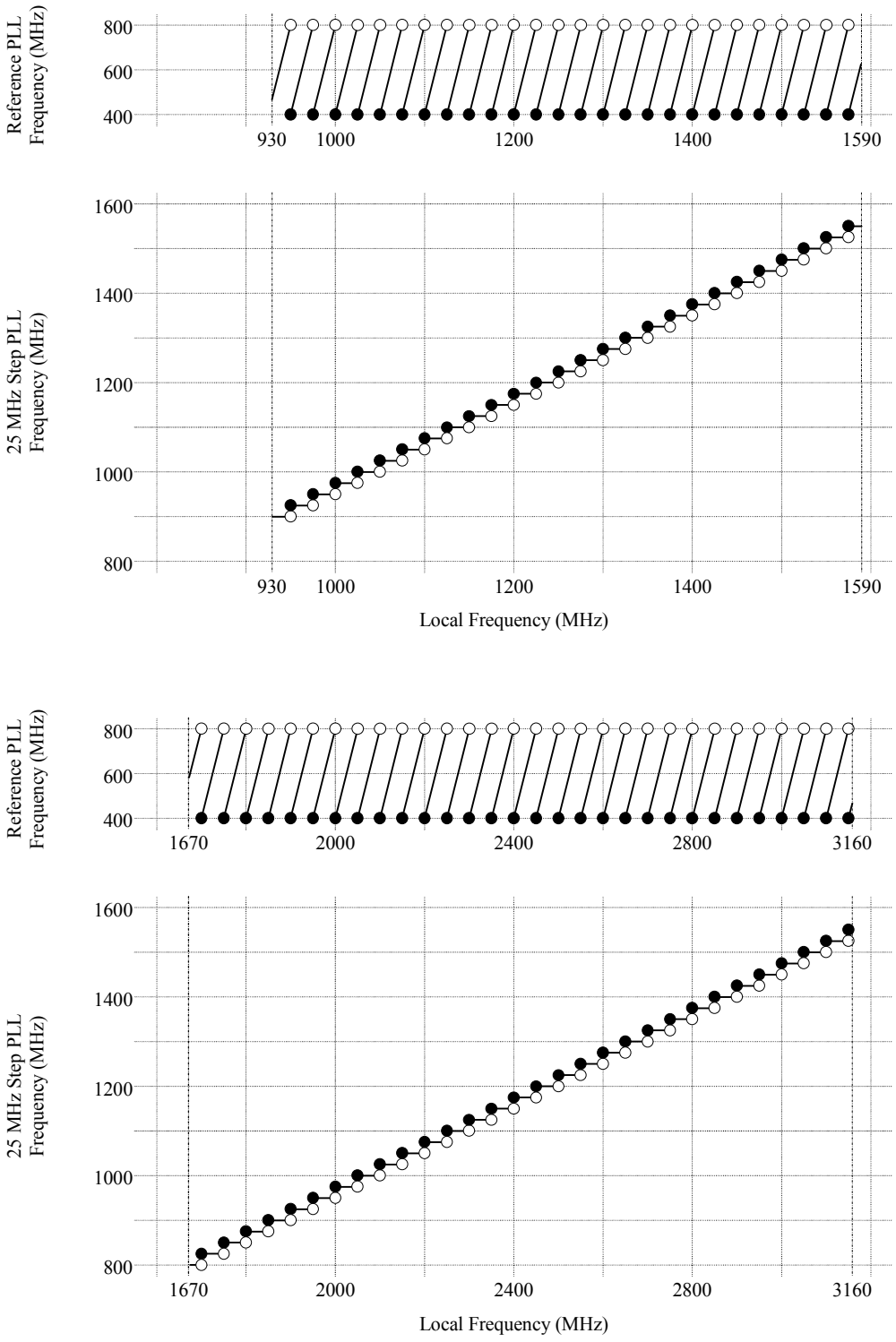


Fig.2-13 Local frequency vs 25 MHz Step PLL and Reference PLL frequency

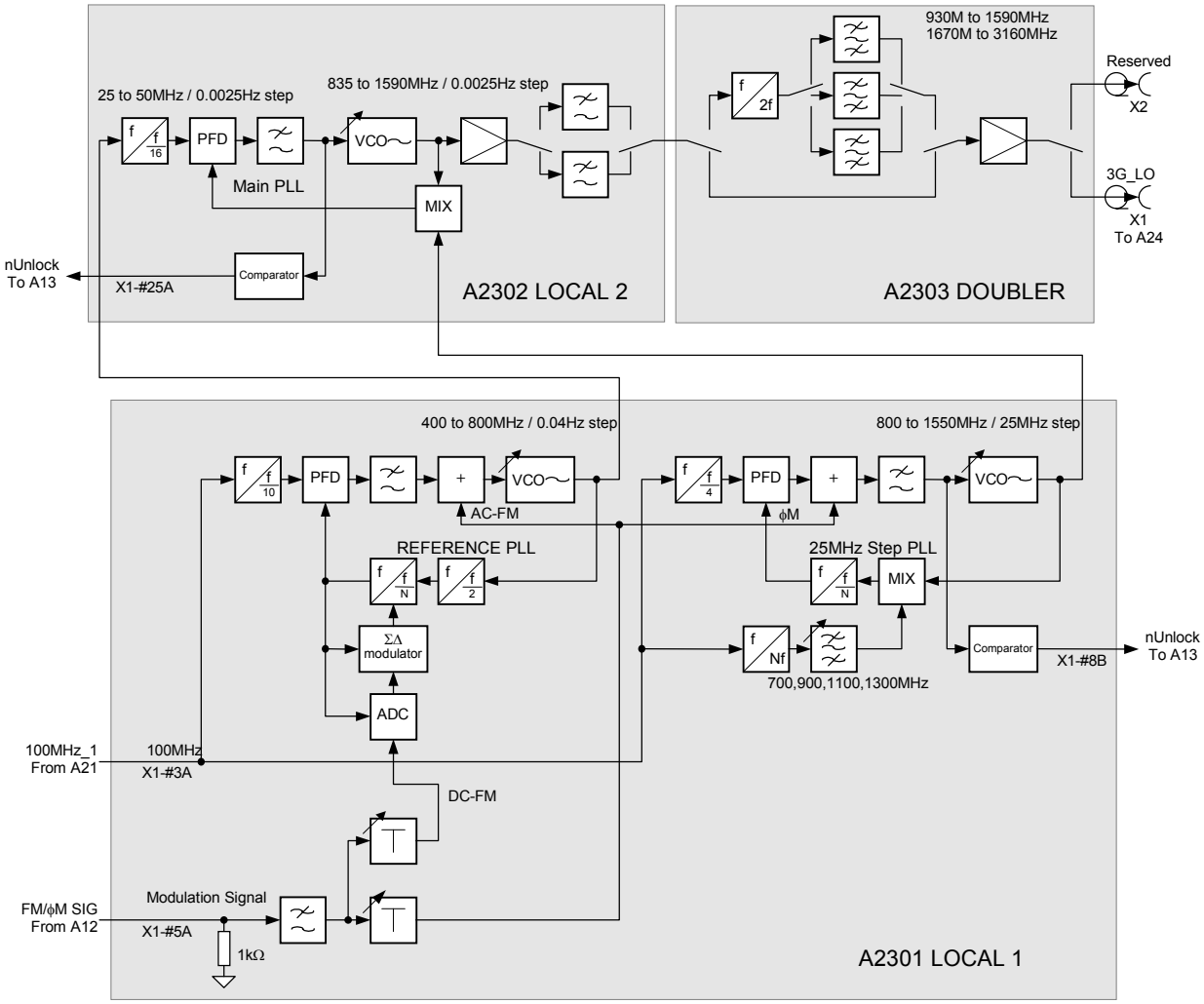


Fig.2-14 A23 LOCAL UNIT Block Diagram

2.2.13 A24 3G RF UNIT

The A24 3G RF UNIT, structured in an aluminum-shielded case, is inserted in the top of the equipment. It mixes the IF signal fed from the A22 I/Q MOD UNIT and the local signal fed from the A23 LOCAL UNIT to convert the signal mix to an output frequency so as to generate a final output signal.

The A24 3G RF UNIT is built of five PC boards and a BPF modules. The A2401 3G MIXER mixes the IF signal fed from the A22 I/Q MOD UNIT and the local signal fed from the A23 LOCAL UNIT to convert them into an output frequency. Since this signal contains a greater proportion of spurious signals, such as image signals resulting from mixing and local leak signals, it is passed through a filter module chosen from A2403 3G FILTER 1 or A2404 3G FILTER 2 to suit the output frequency.

The signal removed of spurious contents through filtering is amplified by the A2402 3G AMP to a required level and then generated from the front-panel RF Output connector via the S-ATT&RPP.

The signal output from the output amplifier is detected by the detector and returned to the A22 I/Q MOD UNIT as an ALC circuit monitor signal.

The A2405 3G CONT feeds a control signal and power to other PC boards.

Figure 2-15 shows the output level of the A24 3G RF UNIT associated with the output level setting. Figure 2-16 shows a block diagram of the A24 3G RF UNIT.

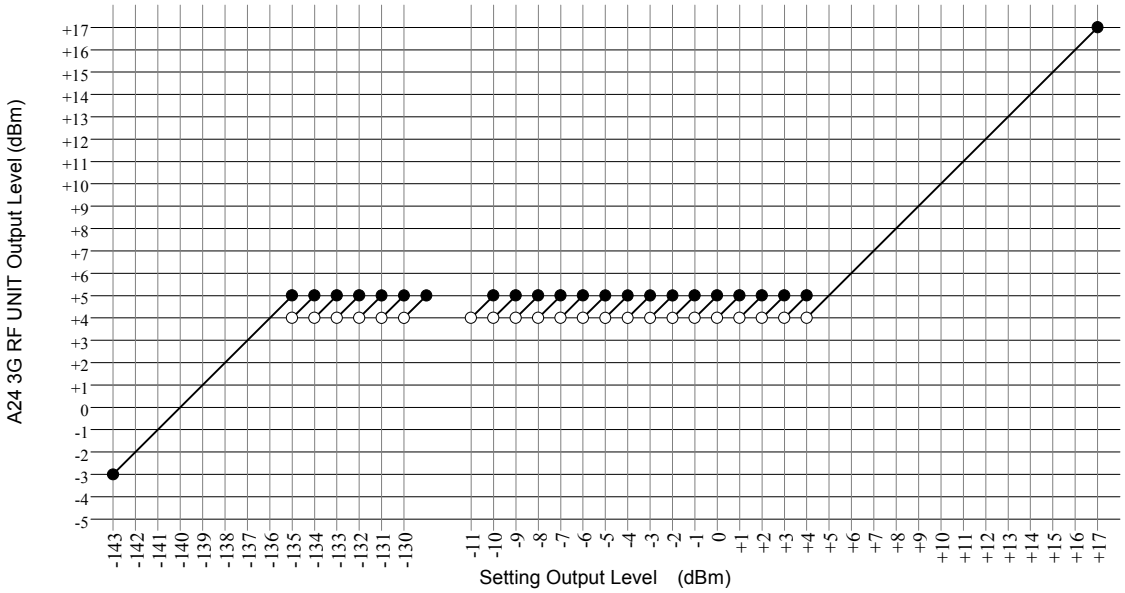


Fig.2-15 Setting Output Level vs. A24 3G RF UNIT Output Level

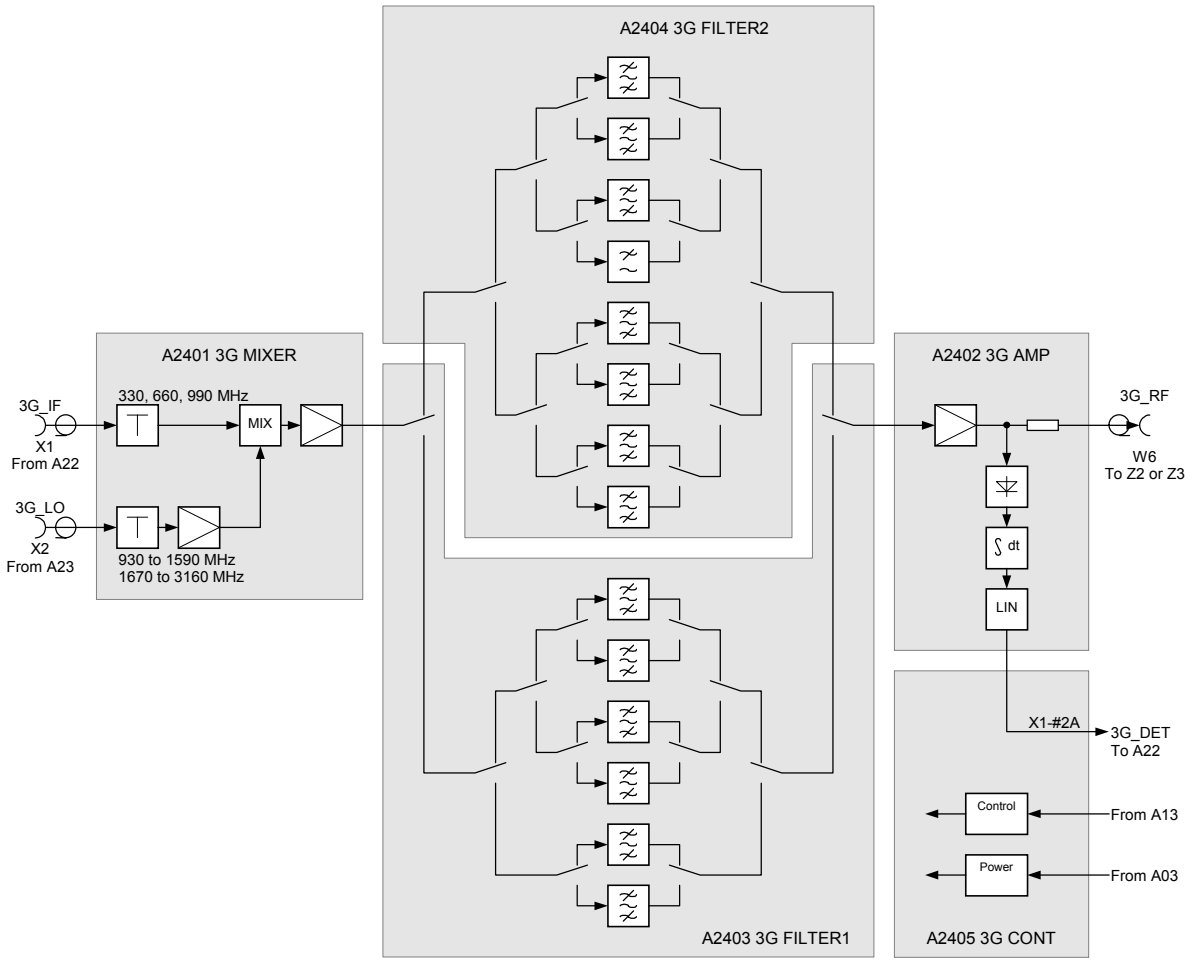


Fig.2-16 A24 3G RF UNIT Block Diagram

2.2.14 A26 POWER AMP UNIT

A26 POWER AMP UNIT is an aluminum-chassis unit installed in the upper-side of the equipment, which is to be installed when adding Option 42 RF High Level Output.

A26 POWER AMP UNIT is to be inserted between the output of A24 3G RF UNIT and the input of Z2 ATT&RPP. A26 POWER AMP UNIT is consists of RF amplifier module and RF coax switch, and toggles between the through route and amplifier route according to the setting from the panel. Figure 2-17 shows the block diagram of A26 POWER AMP UNIT.

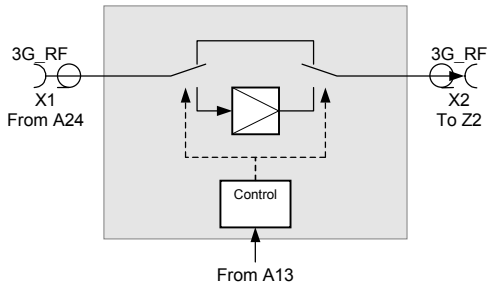


Fig.2-17 A26 POWER AMP UNIT Block Diagram

SECTION 3
TROUBLESHOOTING

3.1 Outline

This section provides instructions on how to locate faults occurring in the MG3681A.

3.2 Explanation of Identification Markings on the PC Board

As shown in Figure 3-1, the PC board mounted in this equipment is marked with a PC board number (with a revision number), a PC board name, and a test point name.

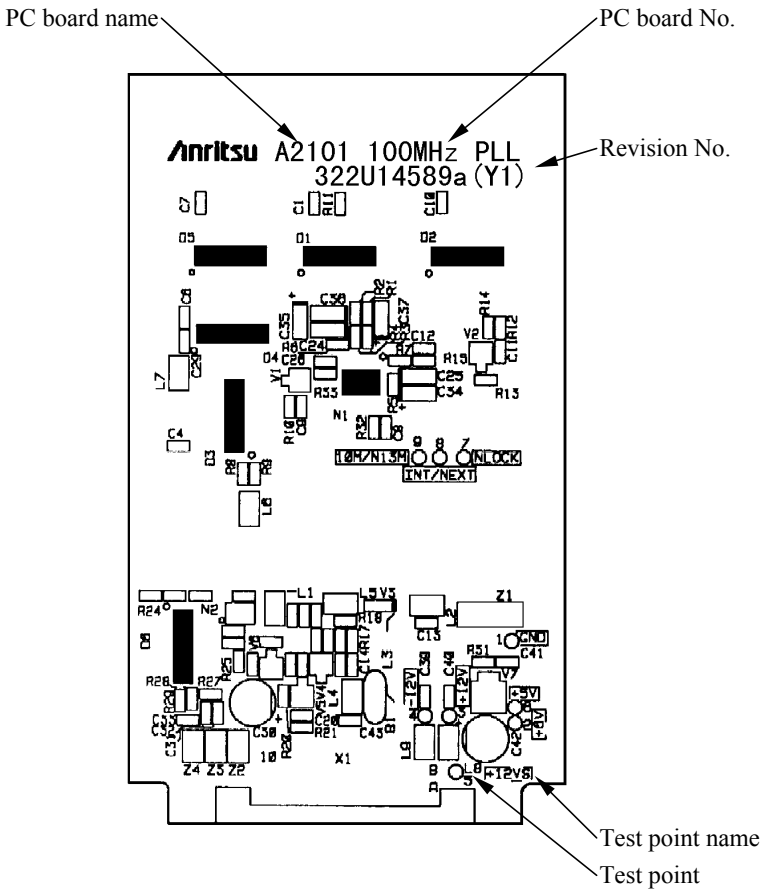


Fig. 3-1 PC Board Identification Markings

3.3 Service Kit

Table 3-1 describes the contents of the service kit that is sold separately. The order number of this service kit is 34Y125569.

Table 3-1 Service Kit (Sold separately)

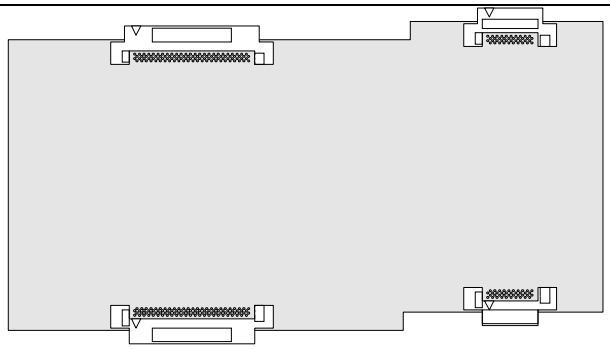
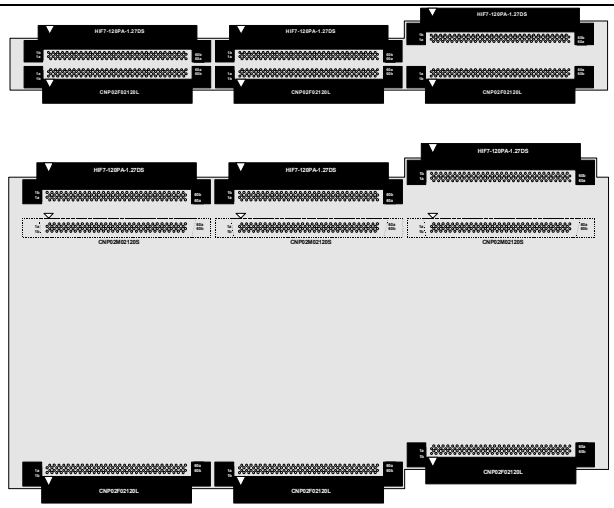
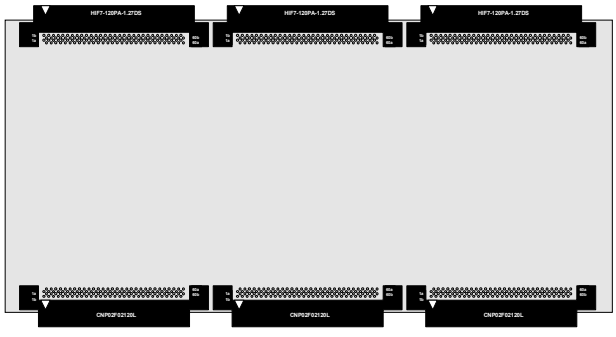
No.	Dwg.No	Accessory Name	Q'ty	Remarks
1	349J122236	Extender for AUDIO/CLOCK	1	
2	349J122237	Extender for MAIN CPU	1	
3	349J122238	Extender for DIGITAL BOARD	1	

Table 3-1 Service Kit (Sold separately) (continued)

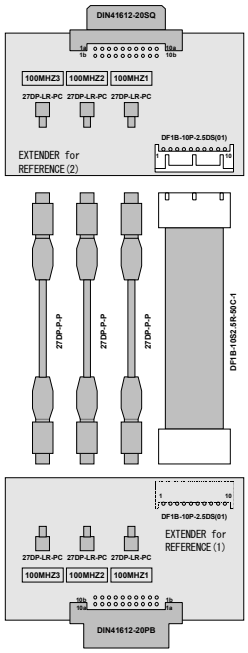
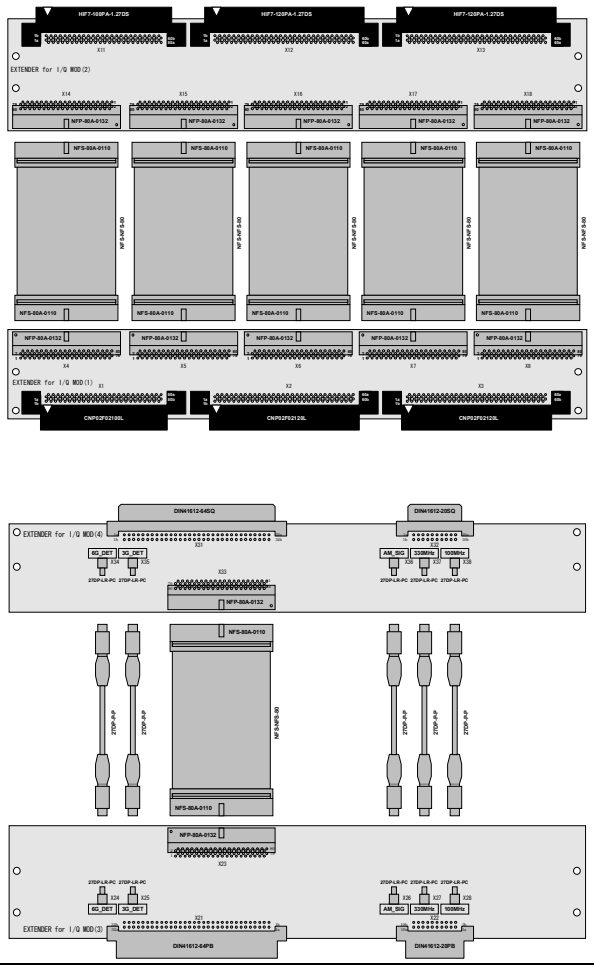
No.	Dwg.No	Accessory Name	Q'ty	Remarks
4	349J122239	Extender for REFERENCE	1	
5	349J122240	Extender for I/Q MOD	1	

Table 3-1 Service Kit (Sold separately) (continued)

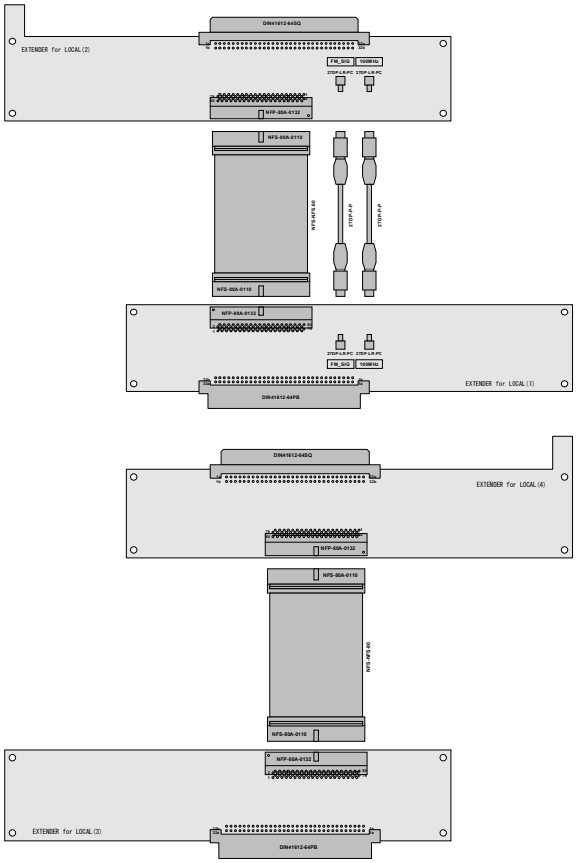
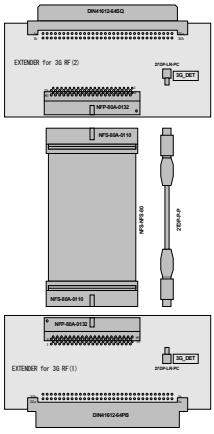
No.	Dwg.No	Accessory Name	Q'ty	Remarks
6	349J122241	Extender for LOCAL	1	
7	349J122242	Extender for 3G_RF	1	

Table 3-1 Service Kit (Sold separately) (continued)

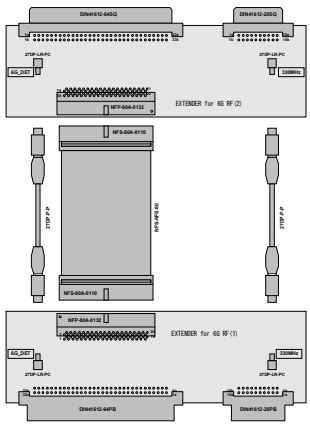
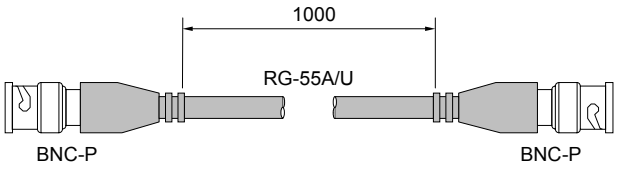
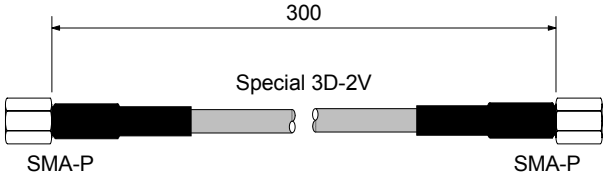
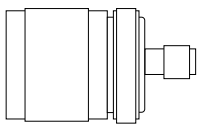
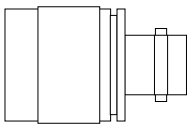
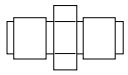
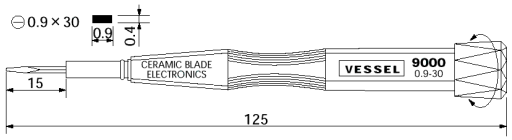
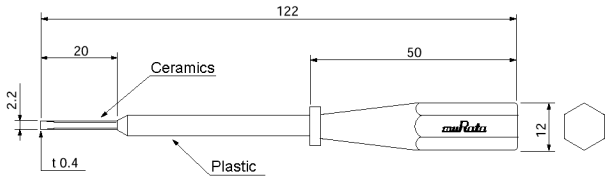
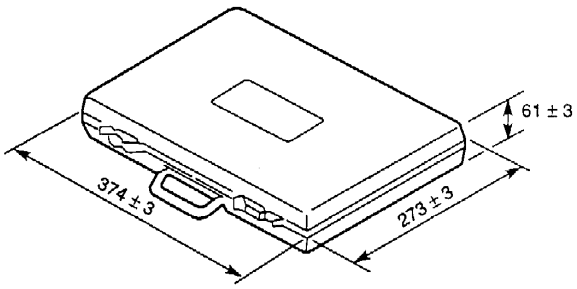
No.	Dwg.No	Accessory Name	Q'ty	Remarks
8	349J122243	Extender for 6G_RF	1	
9	34J103624F	Extender Cable	5	
10	S4J10001B	Extender Cable	5	
11	S4W10184C	Extender Cable	4	
12	S4J10319	NP-SMAJ (SMA-AD12-SF(12)) Adaptor	1	
13	No.1305	NP-BNCJ (JUG-201A/U) Adaptor	1	

Table 3-1 Service Kit (Sold separately) (continued)

No.	Dwg.No	Accessory Name	Q'ty	Remarks
14	S4J10319	SMAJ-SMAJ (SMA-AD5-SF(12)) Adaptor	2	
15	No.1268	Adjustment Driver	1	
16	No.1268	Adjustment Driver	1	
17	34B35154	Torque Wrench	1	
18	343Z130587	Carrying Case	1	
19	343Z130587B	Carrying Case	1	
20	343Z130587C	Carrying Case	1	

3.4 Instruments Required for Troubleshooting

Table 3-2 lists the instruments that are required for troubleshooting.

Table 3-2 Instruments Required for Troubleshooting

Instrument (Anritsu)	Major Performance
Frequency Counter (MF1603A)	100 kHz to 6 GHz
Spectrum Analyzer (MS2602A)	100 kHz to 8.5 GHz
AC/DC Volt Meter	AC : 250 V, DC : ±50 V
Oscilloscope	DC to 100 MHz
Power Meter (ML4803A.MA4601A)	100 kHz to 6 GHz
Calibration Receiver (ML2530A)	100 kHz to 3 GHz
Modulation Analyzer (MS616B)	100 kHz to 3 GHz, AM, FM
Function Generator	10 Hz to 1 MHz, 0 to 2 Vp-p / 600 Ω, 50 Ω
Personal Computer	IBM PC/AT Compatible, Windows 95 / 98
GPIB Interface	National Instruments PCI-GPIB or PCMCIA-GPIB interface (NI-488.2^{TM})

3.5 Circuit Reference

The units and PC boards that are mounted in this equipment each have a module name that begins with "MM." The names and module names of these units and PC boards are listed in Table 3-3. They are available by module name.

Table 3-3 Circuit Reference (MG3681A Main Frame)

Module No.	Name	Note
MM300001A	A03 REGULATOR	
MM300002A	A04 KEY ENCODE	
MM300003A	A05 REAR CONNECT	
MM300004A	A12 AUDIO/CLOCK	To be installed with MM300011A
MM300004B	A12 AUDIO/CLOCK	To be installed with MM300011B
MM300005A	A13 MAIN CPU	
MM300006A	A16 POWER SUPPLY UNIT	
MM300007A	A17 FAN ASSY	
MM300008A	A18 FAN ASSY	
MM300010A	A21 REFERENCE UNIT	
MM300011A	A22 I/Q MOD UNIT	To be installed with MM300004A
MM300011B	A22 I/Q MOD UNIT	To be installed with MM300004B
MM300012A	A23 LOCAL UNIT	
MM300013A	A24 3G RF UNIT	
MM300015A	A1101 SWITCH BOARD	
MM300016A	A1102 DISPLAY ASSY	
339H38476	Z2 S-ATT&RPP	
PH-BLC08-K2	U1 BACKLIGHTING INVERTER POWER SUPPLY	

Table 3-4 Circuit Reference (Expansion Units)

Exp. Unit Name	Module No.	Name	Note
MU368040A	MM300017A	A32 CDMA	To be used for equipment installed with MM300011A
	MM300017B	A32 CDMA	To be used for equipment installed with MM300011B
	MM300018A	A33 DIGITAL FILTER	To be used for equipment installed with MM300011A
	MM300018B	A33 DIGITAL FILTER	To be used for equipment installed with MM300011B
MU368010A	MM300019A	A31 TDMA	
MU368060A	MM300022A	A37 C/N CONT	
MU368030A	MM300024A	A38 20Msps ARB	

3.6 Overall Troubleshooting

3.6.1 Outline of Troubleshooting Procedure

Figure 3-5 shows an overview of the flow of troubleshooting process.

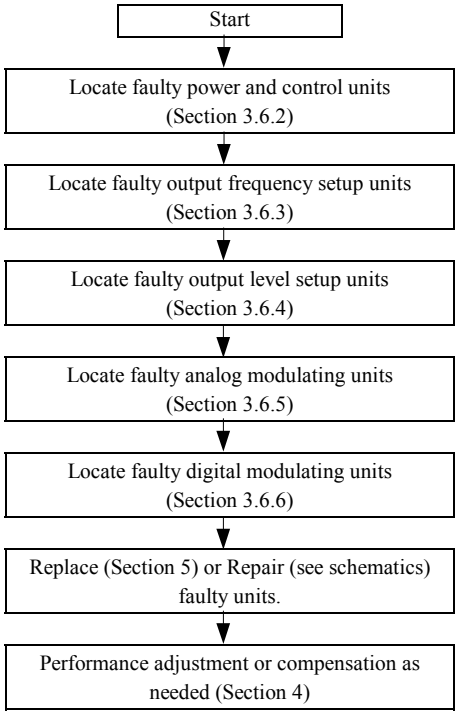


Fig.3-5 Outline of Troubleshooting Procedure

3.6.2 Power and Control Troubleshooting

Figure 3-6 shows Flowchart for locating faulty power and control blocks.

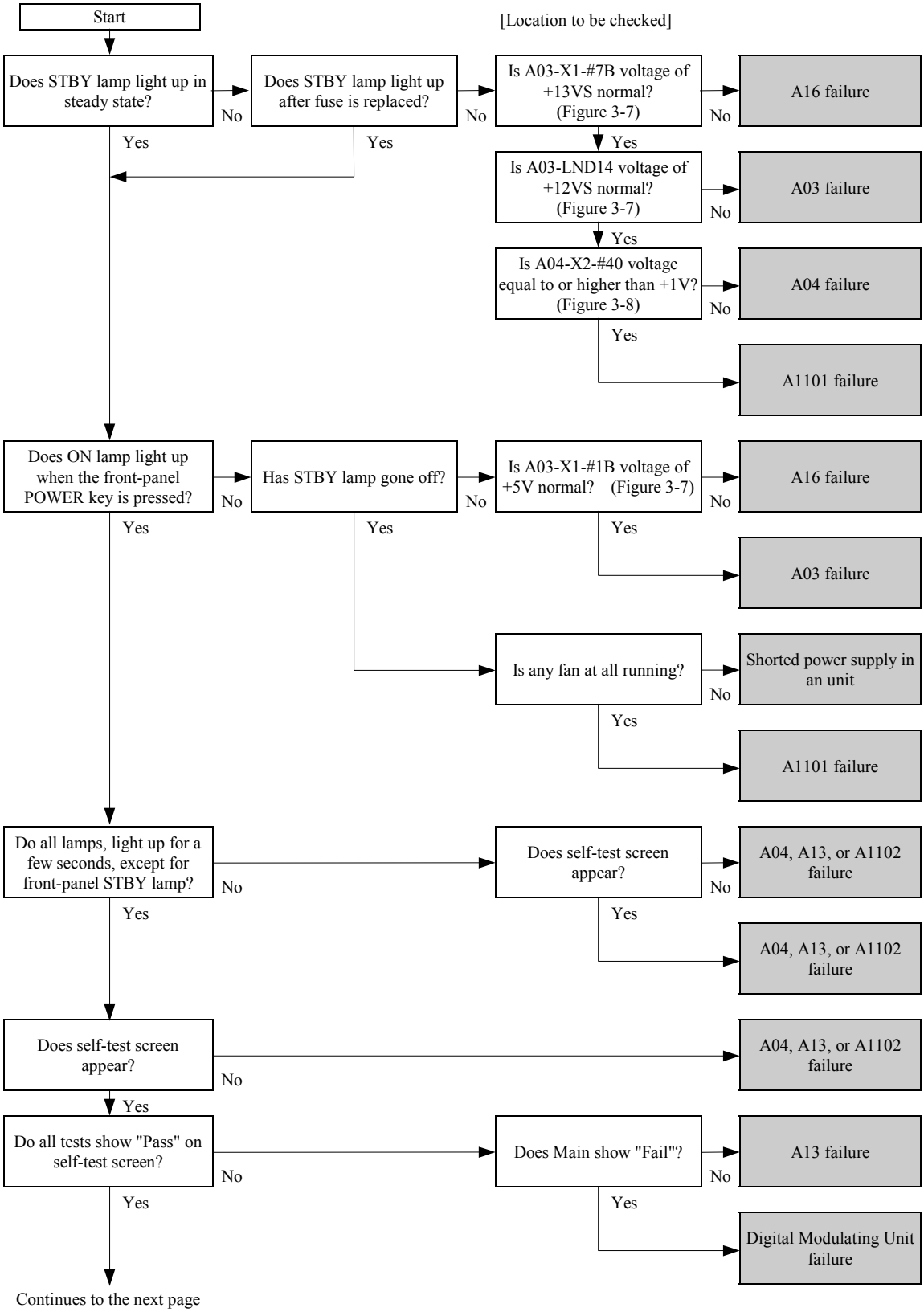


Fig.3-6 Overall Troubleshooting Flowchart (to be continued)

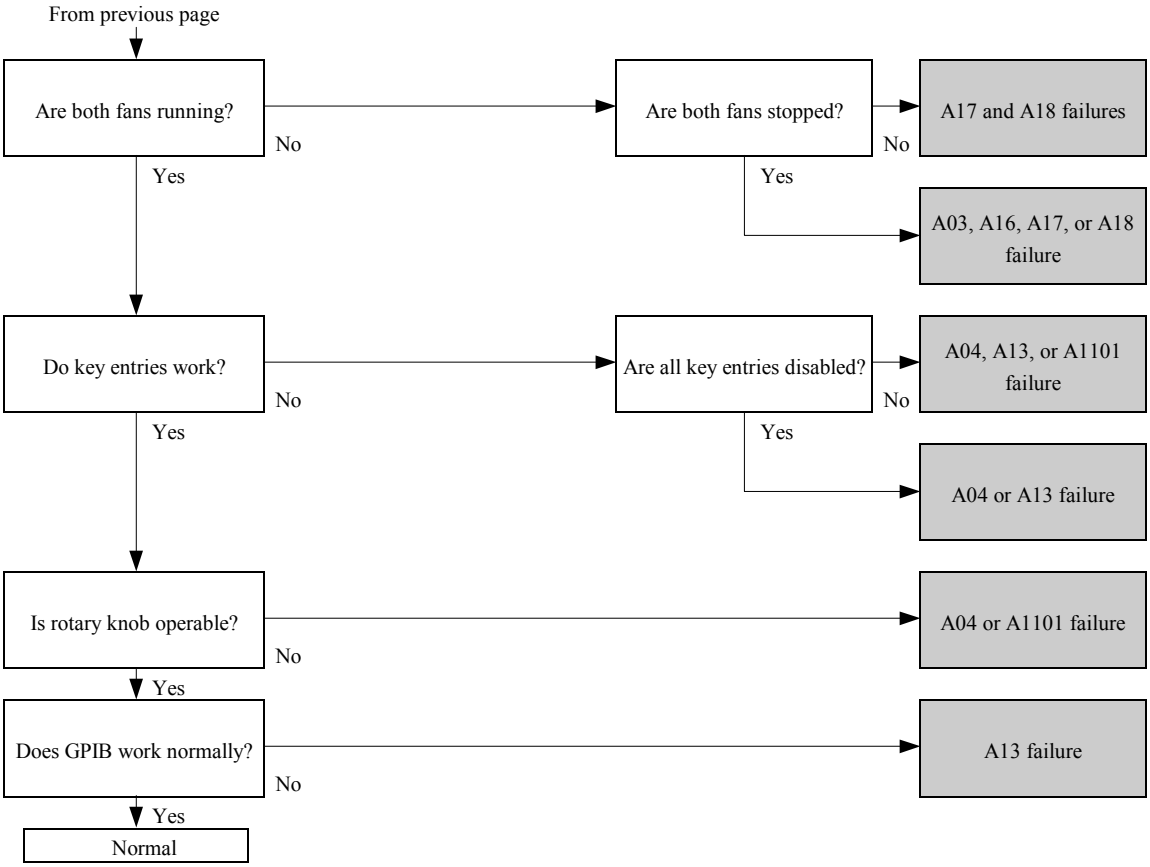


Fig.3-6 Overall Troubleshooting Flowchart (continued)

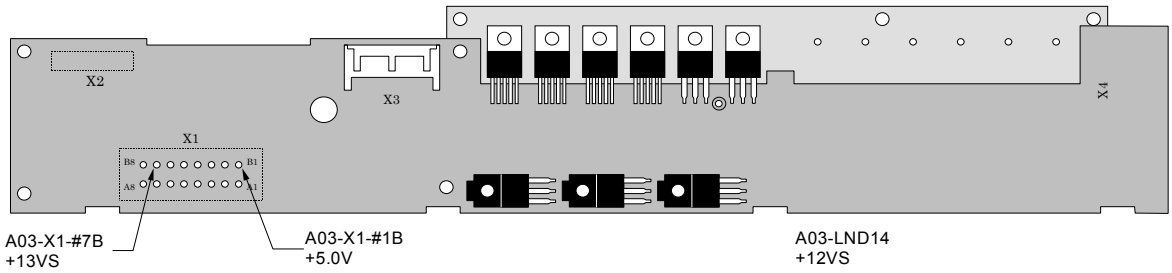


Fig.3-7 Check Points of A03 REGULATOR

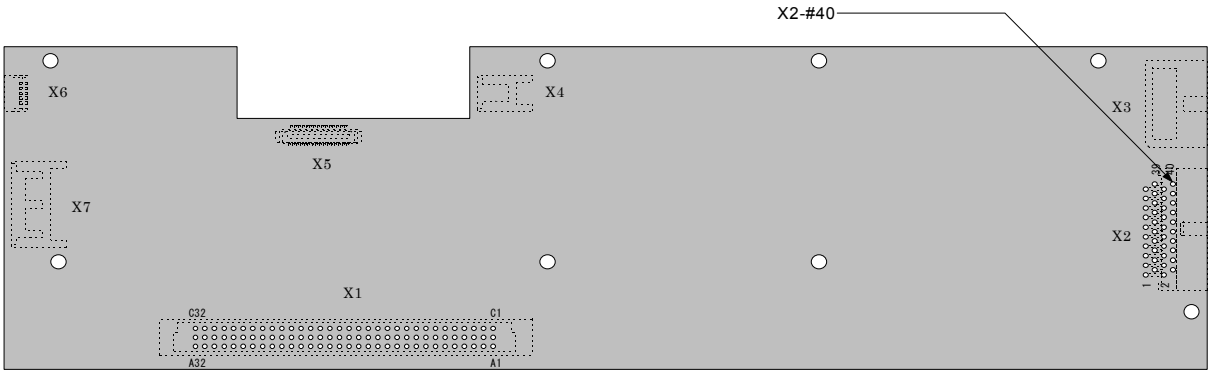


Fig.3-8 Check Points of A04 KEY ENCODE

3.6.3 Output Frequency Troubleshooting

Figure 3-9 shows Flowchart for locating faulty output frequency setup units.

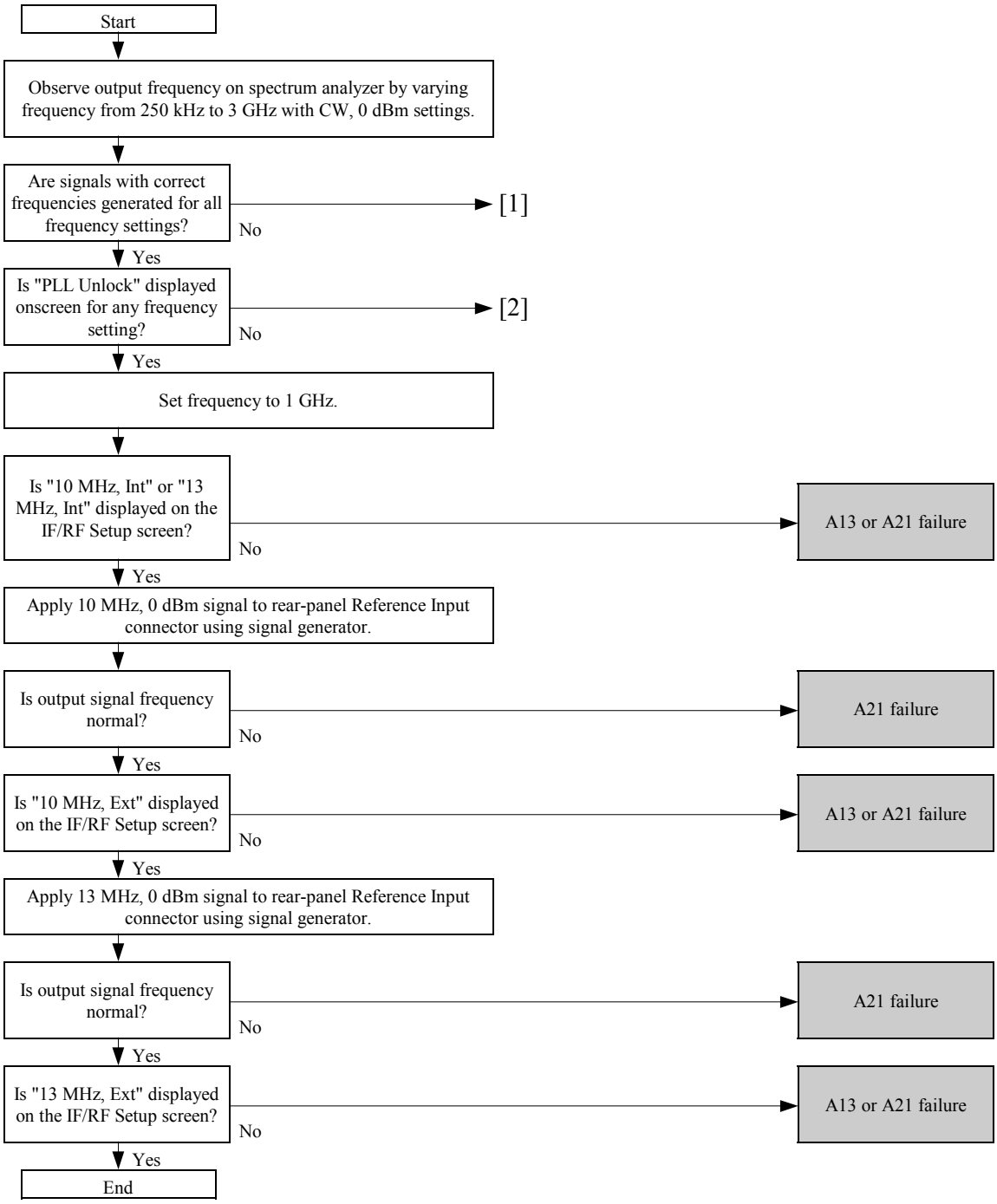


Fig.3-9 Frequency Troubleshooting Flowchart (to be continued)

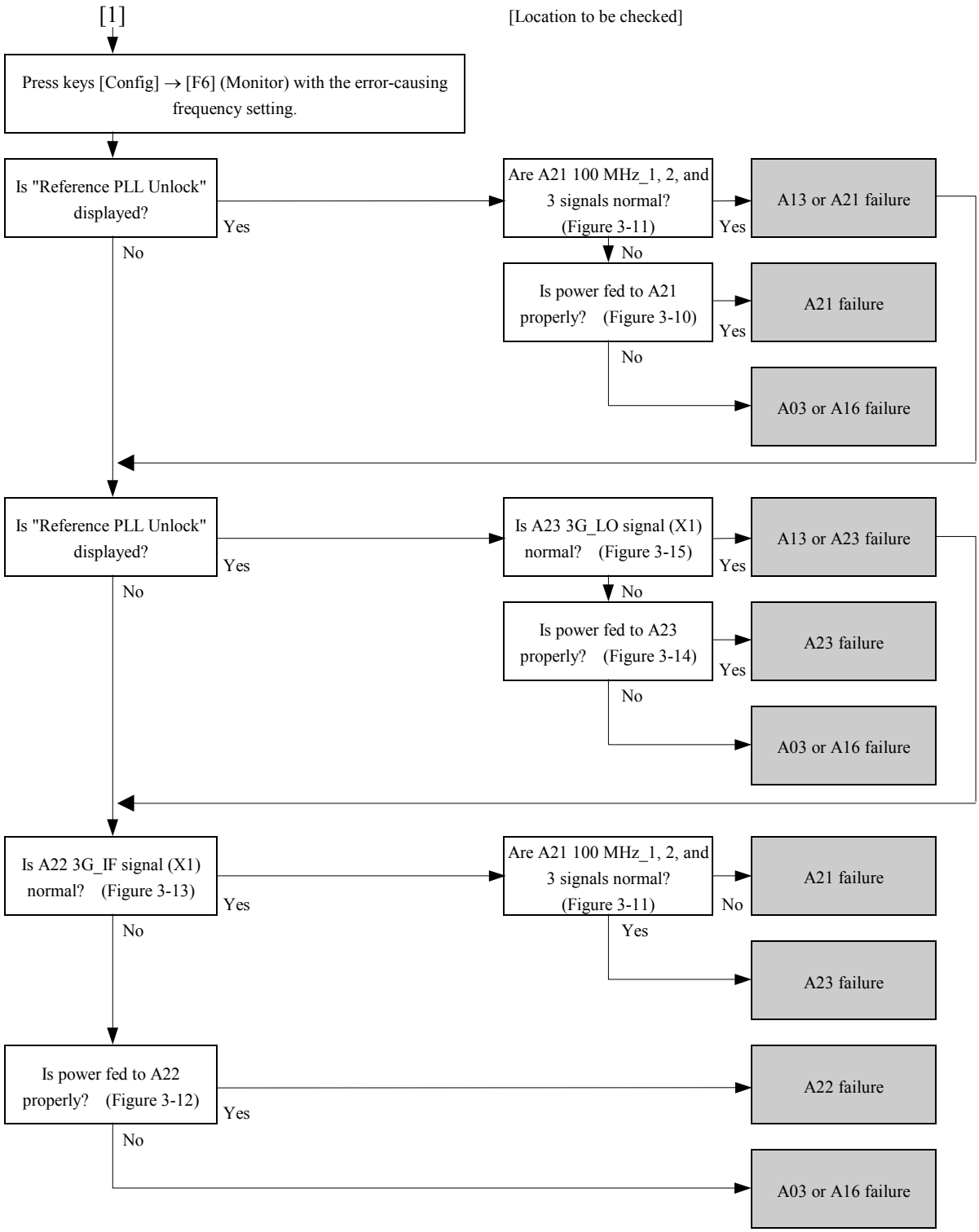


Fig.3-9 Frequency Troubleshooting Flowchart (to be continued)

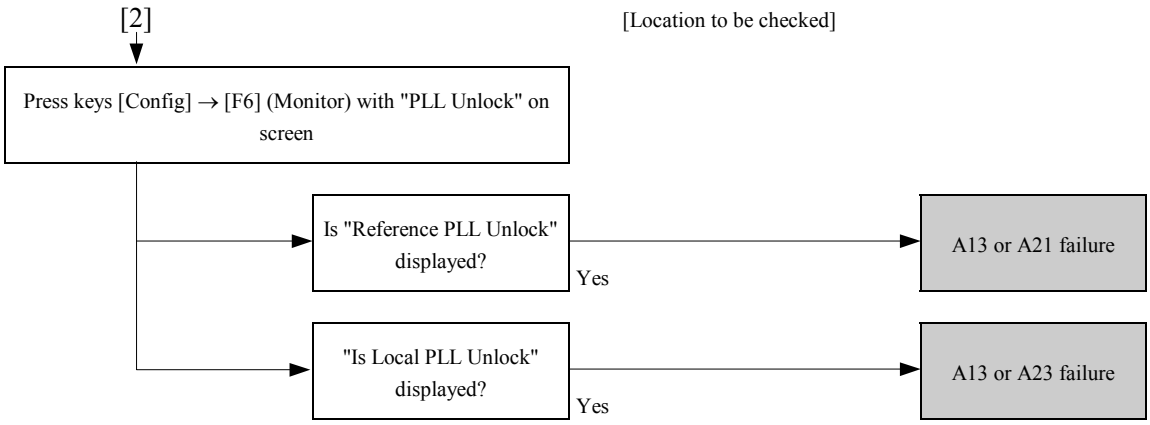


Fig.3-9 Frequency Troubleshooting Flowchart (continued)

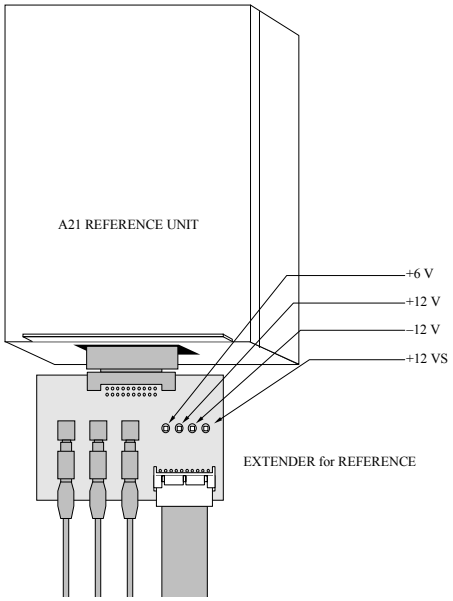


Fig.3-10 Power Check Point of A21 REFERENCE UNIT

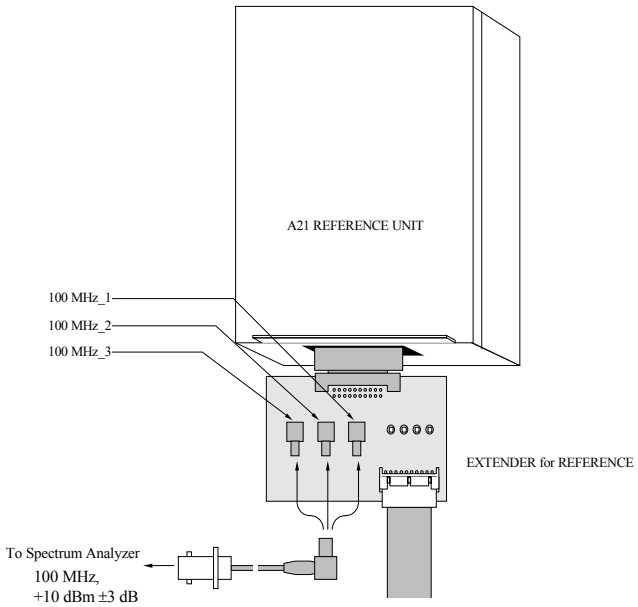


Fig.3-11 Signal Check Point of A21 REFERENCE UNIT

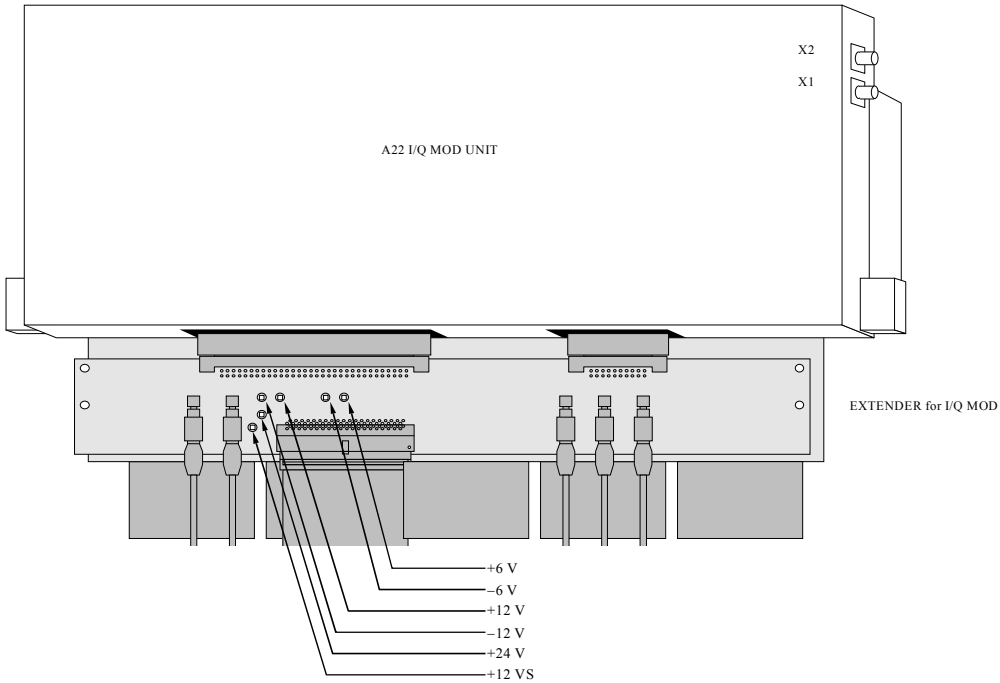


Fig.3-12 Power Check Point of A22 I/Q MOD UNIT (A2221 IF GENERATOR)

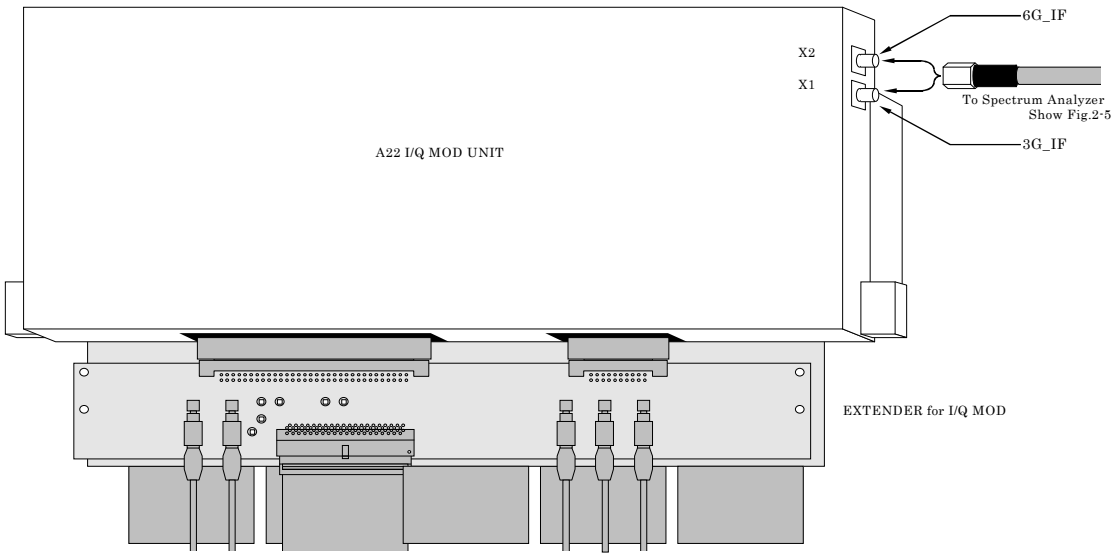


Fig.3-13 Signal Check Point of A22 I/Q MOD UNIT (A2221 IF GENERATOR)

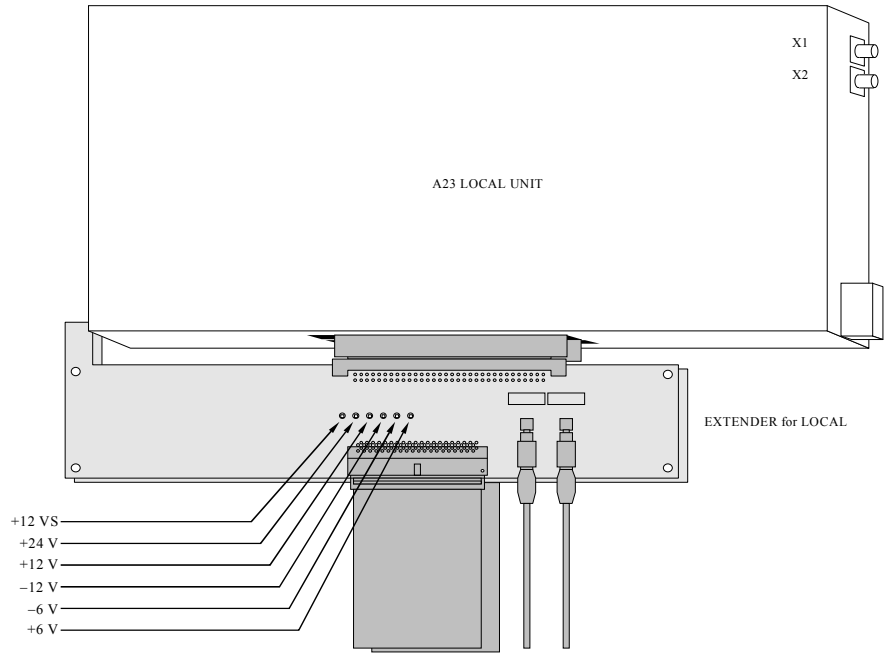


Fig.3-14 Power Check Point of A23 LOCAL UNIT

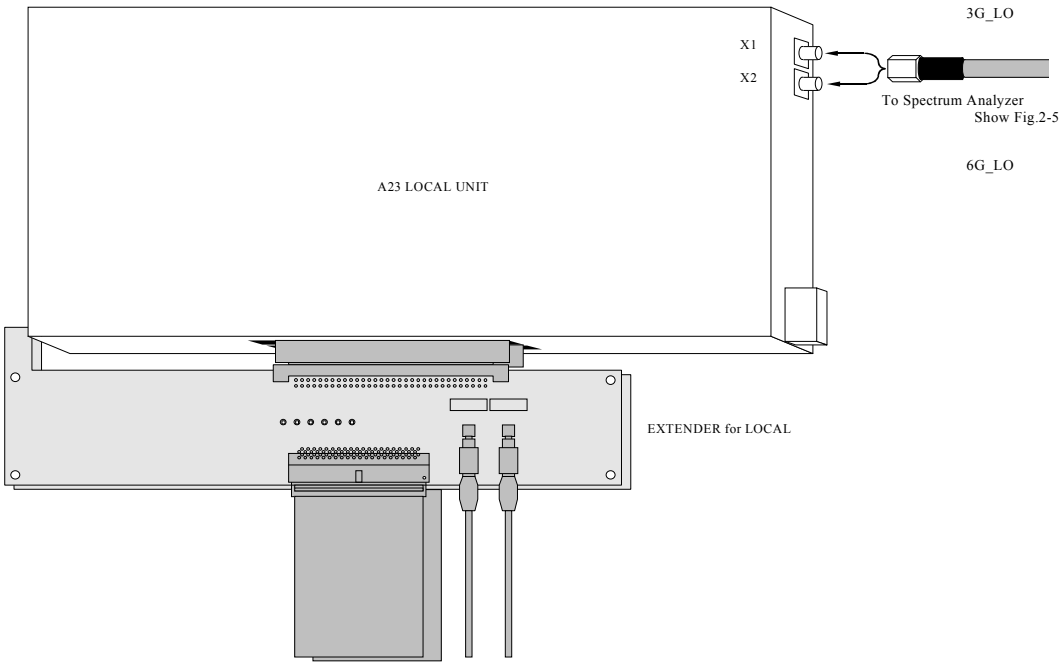


Fig.3-15 Signal Check Point of A23 LOCAL UNIT

3.6.4 Output Level Troubleshooting

Figure 3-16 shows Flowchart for locating faulty output level setup units.

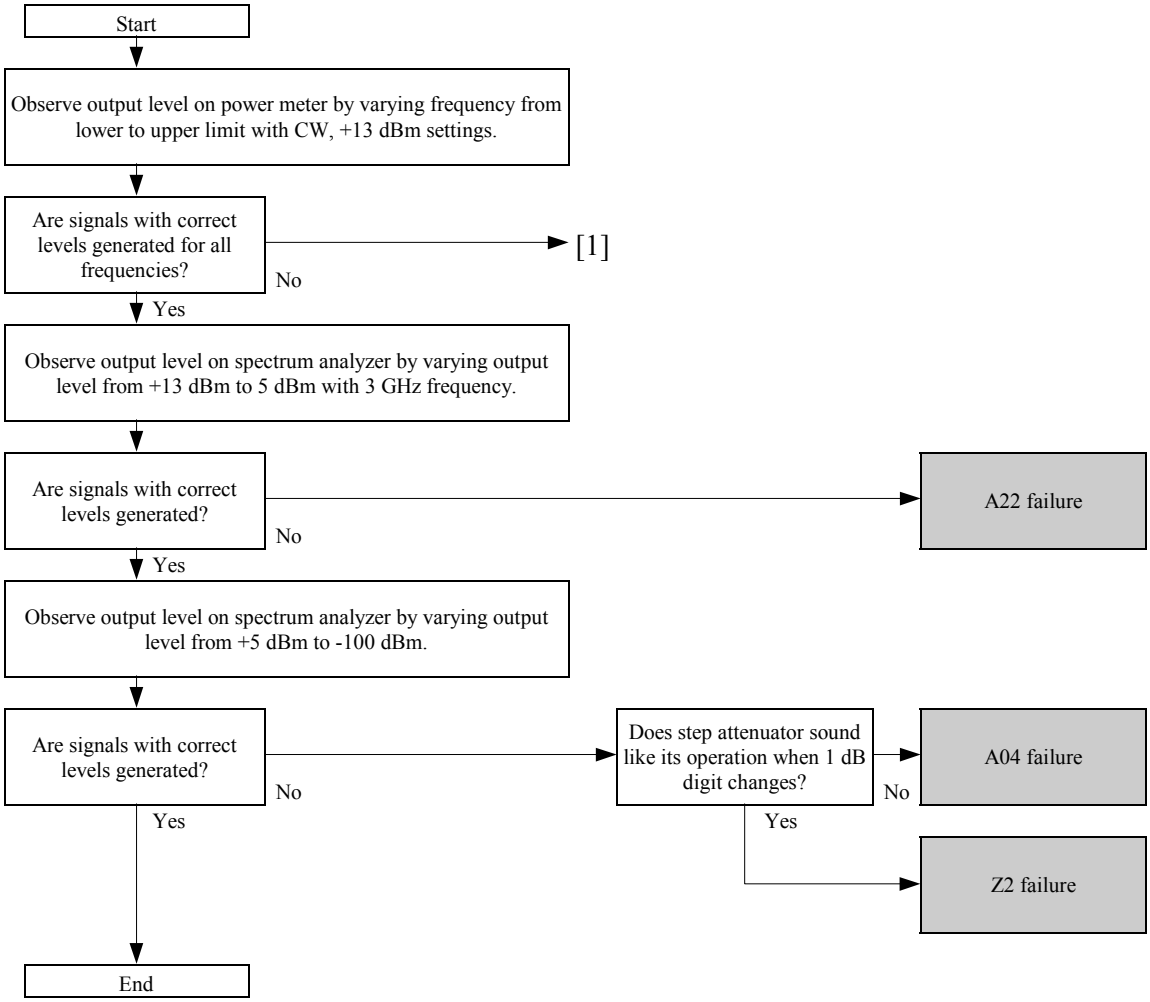


Fig.3-16 Level Troubleshooting Flowchart (to be continued)

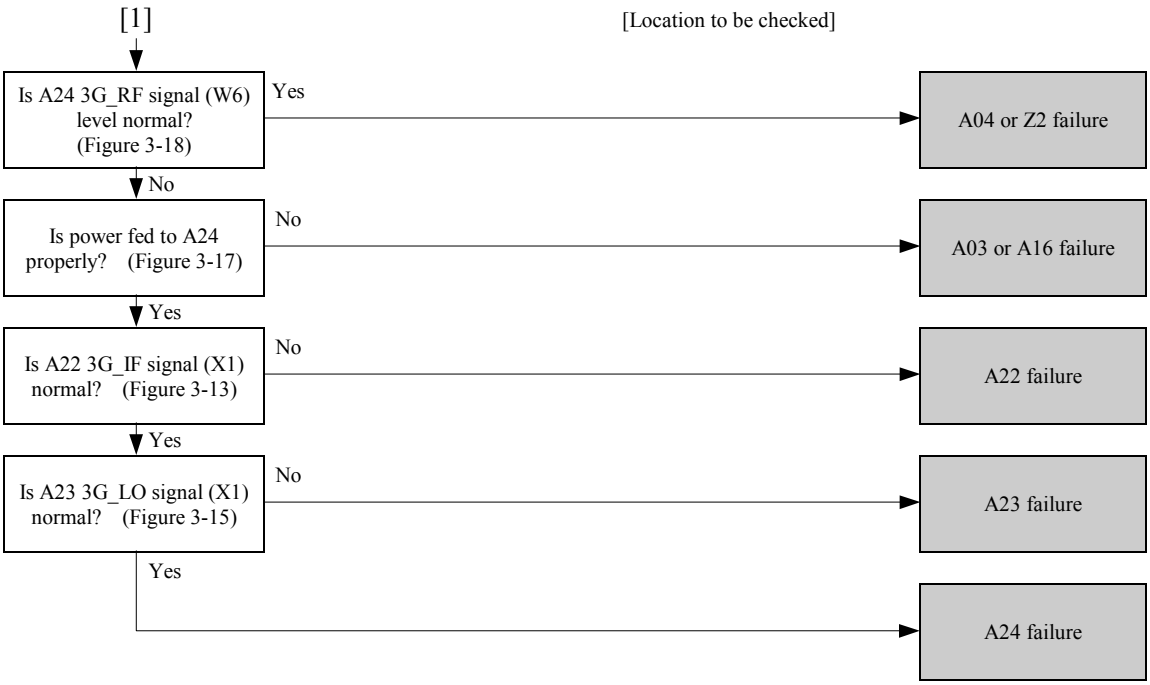


Fig.3-16 Level Troubleshooting Flowchart (continued)

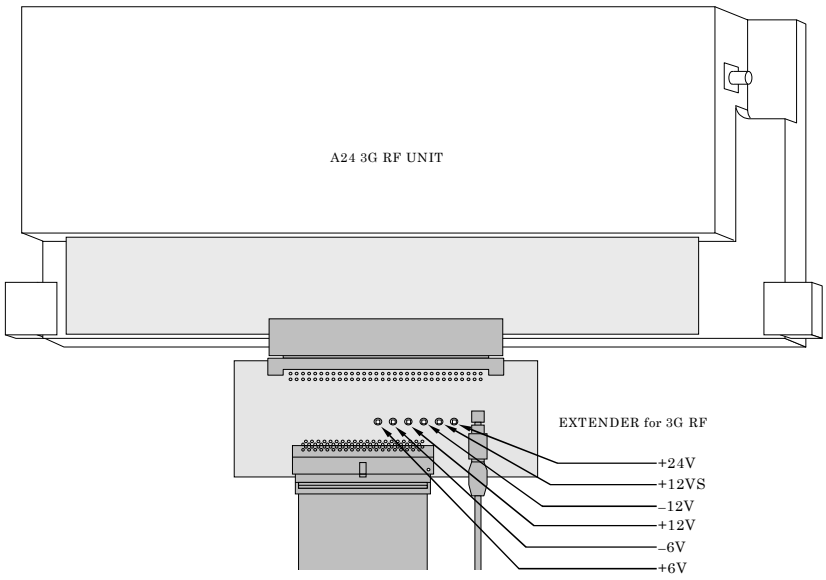


Fig.3-17 Power Check Point of A24 3G RF UNIT

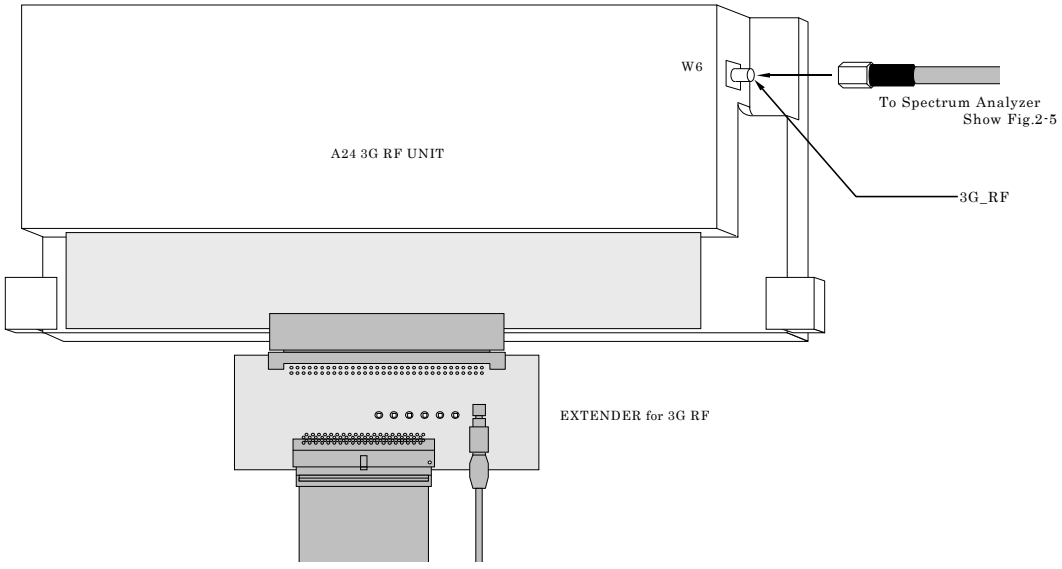


Fig.3-18 Signal Check Point of A24 3G RF UNIT

3.6.5 Analog Modulation Troubleshooting

Figure 3-19 shows Flowchart for locating faulty analog modulation setup units.

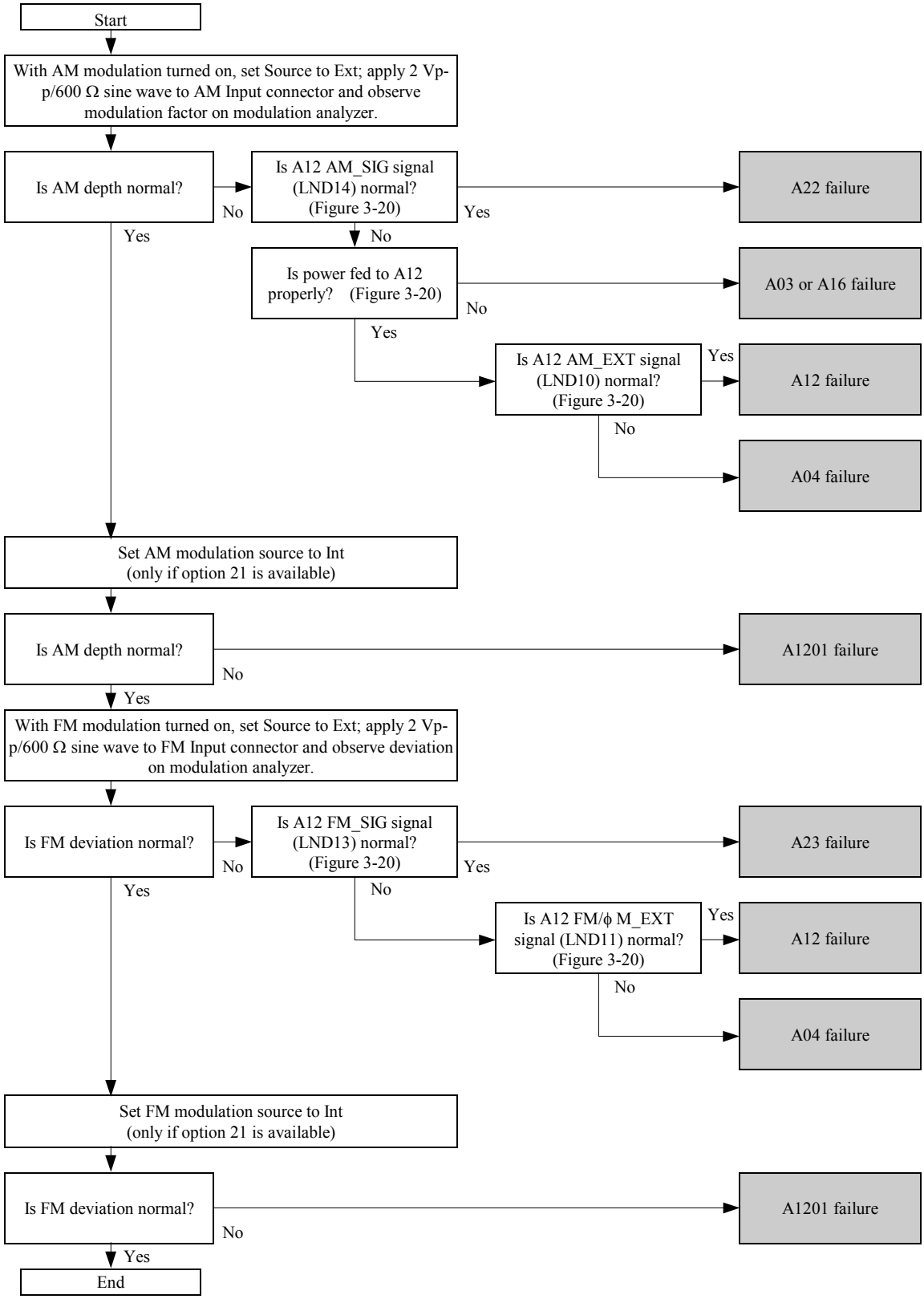


Fig.3-19 Analog Modulation Troubleshooting Flowchart

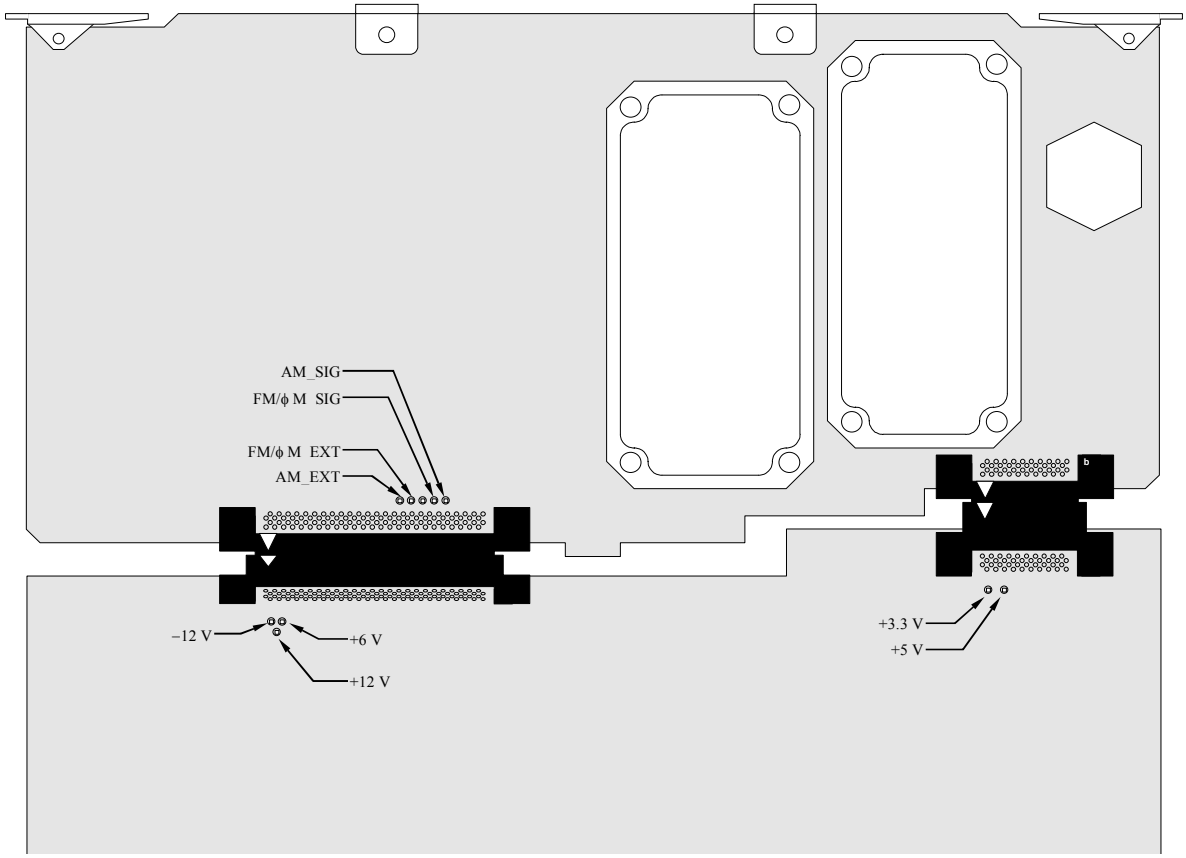


Fig.3-20 Power and Signal Check Point of A12 AUDIO/CLOCK

3.6.6 Digital Modulation Troubleshooting

Figure 3-21 shows Flowchart for locating faulty digital modulation setup units.

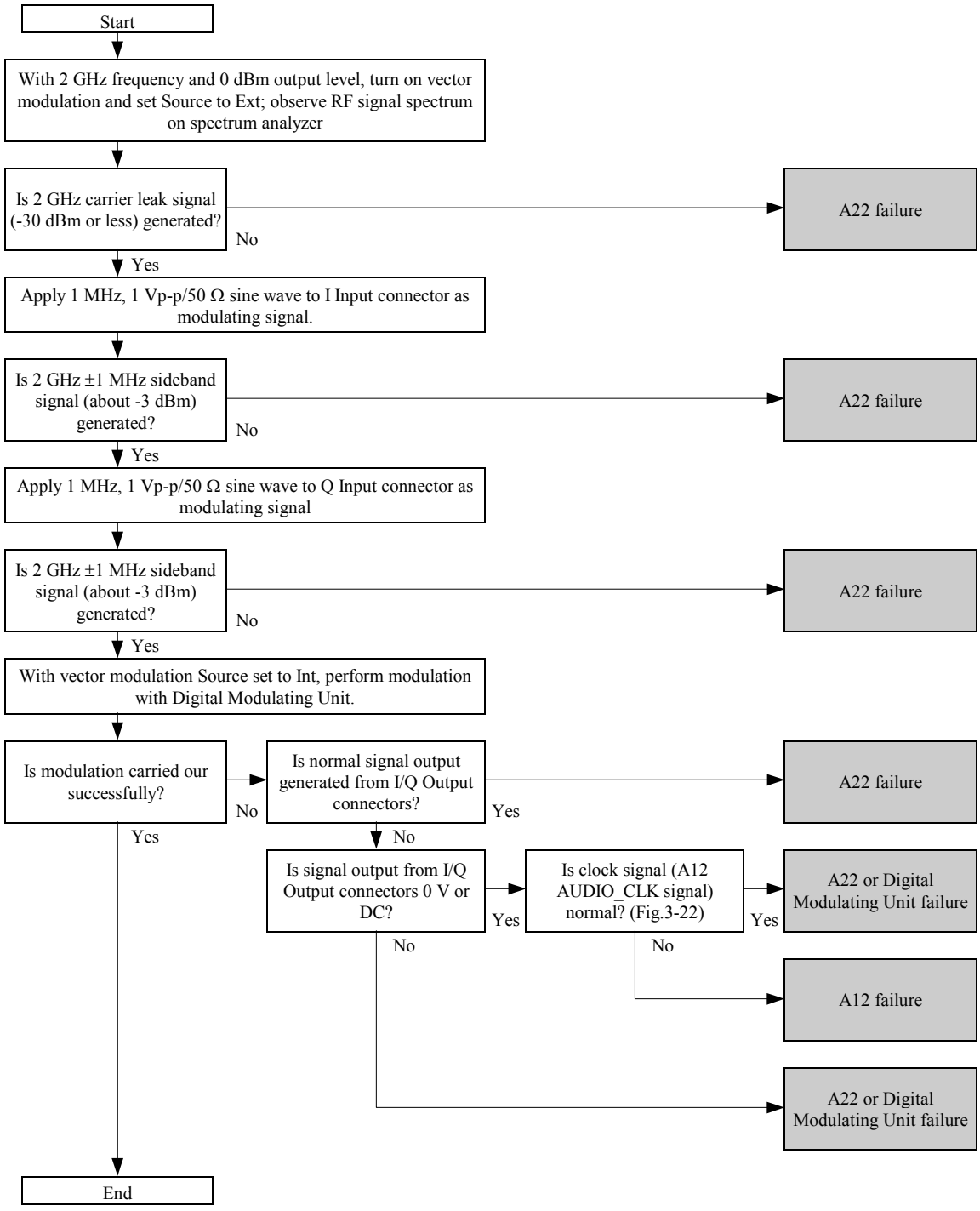


Fig.3-21 Digital Modulation Troubleshooting Flowchart

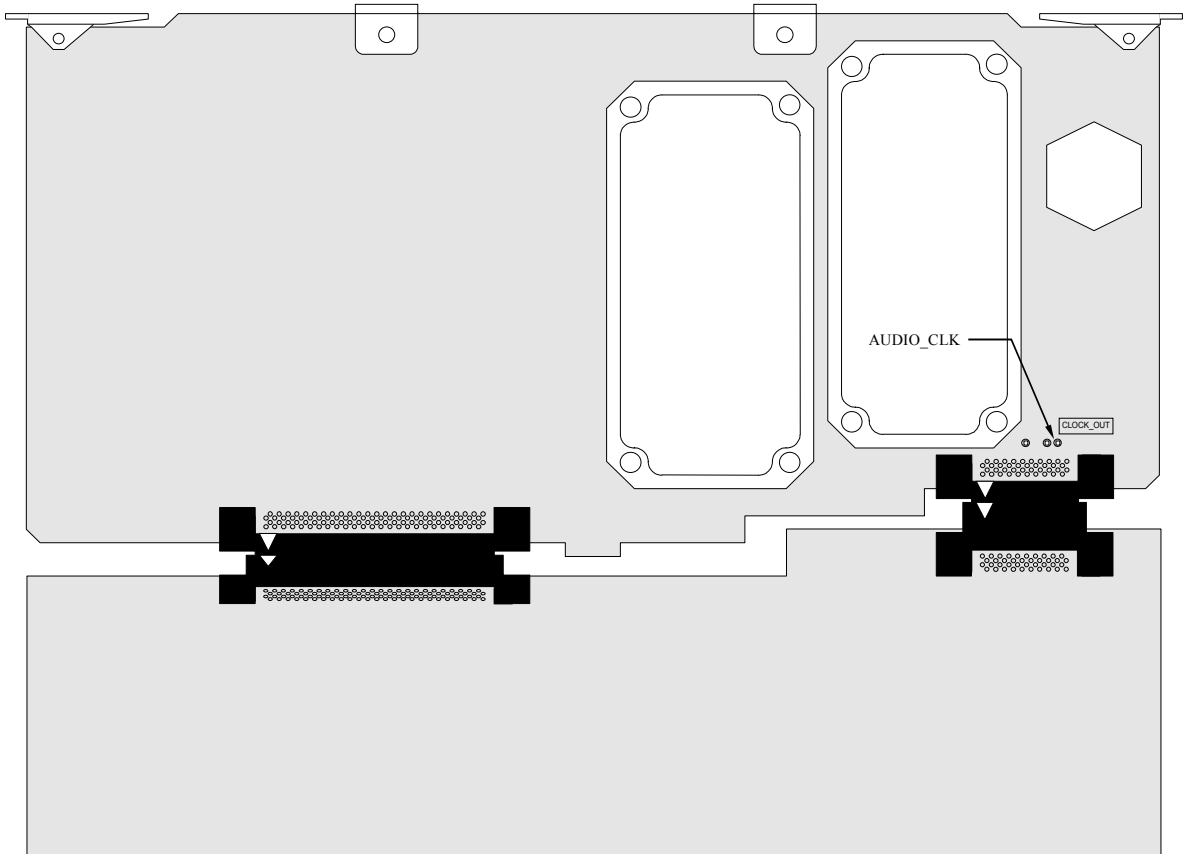


Fig.3-22 Clock Signal Check Point of A12 AUDIO/CLOCK

3-24.

SECTION 4
ADJUSTMENT AND COMPENSATION

4.1 Outline

This section provides instructions on how to adjust and compensate for the signal generator upon completion of troubleshooting. Table 4-1 lists the items of adjustment and compensation required for units that have been either repaired or replaced.

Table 4-1 Items of Adjustment and Compensation After Module Replacement or Repairs

Module	Adjustment and Compensation Item
A22 I/Q MOD UNIT	Vector modulator adjustment (Section 4.3) → Output level compensation (Section 4.4)
A23 LOCAL UNIT	Not required
A24 3G RF UNIT	Output level compensation (Section 4.4)
Z2 S-ATT&RPP	Output level compensation (Section 4.4) → S-ATT&RPP counter reset (Section 4.5)

4.2 Instruments Required for Adjustment and Compensation

Table 4-2 lists the instruments required for adjustment and compensation.

Table 4-2 Instruments Required for Adjustment and Compensation

Instrument	Model Name	Manufacture	Major Performance
Spectrum Analyzer	MS2602A	Anritsu	100 kHz to 8.5 GHz
Power Meter	ML4803A	Anritsu	
Power Sensor	MA4601A	Anritsu	100 kHz to 6 GHz
Calibration Receiver	ML2530A	Anritsu	100 kHz to 3 GHz
Attenuator	MP721B	Anritsu	100 kHz to 8 GHz, 6 dB
Personal Computer			IBM PC/AT Compatible, OS : Windows 95 / 98
GPIB Interface	PCI-GPIB or PCMCIA-GPIB	National Instruments	NI-488.2™
Level Compensation Software			

4.3 Vector Modulator Adjustment

The Vector Modulator in the A22 I/Q MOD UNIT requires adjustment in its mounted condition. Two adjustment items involved are image rejection and carrier leak. The output level would require recompensation when the following unit has been replaced:

· A22 I/Q MOD UNIT

(1) Setup

As shown in Figure 4-1, connect the MG3681A RF Output connector and the Spectrum Analyzer RF Input connector with a coaxial cable.

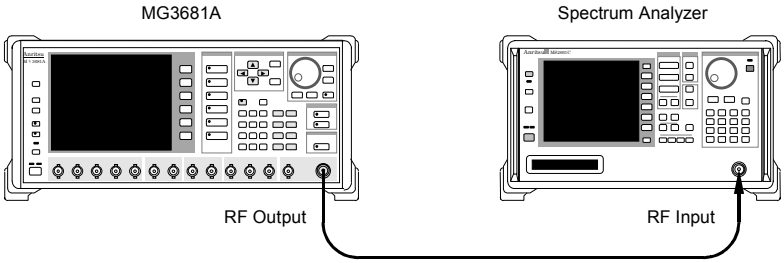


Fig.4-1 Setup

[1] Press the [Preset] key to a preset the Signal Generator.

[2] Set it to a 2 GHz frequency and a 0 dB output level.

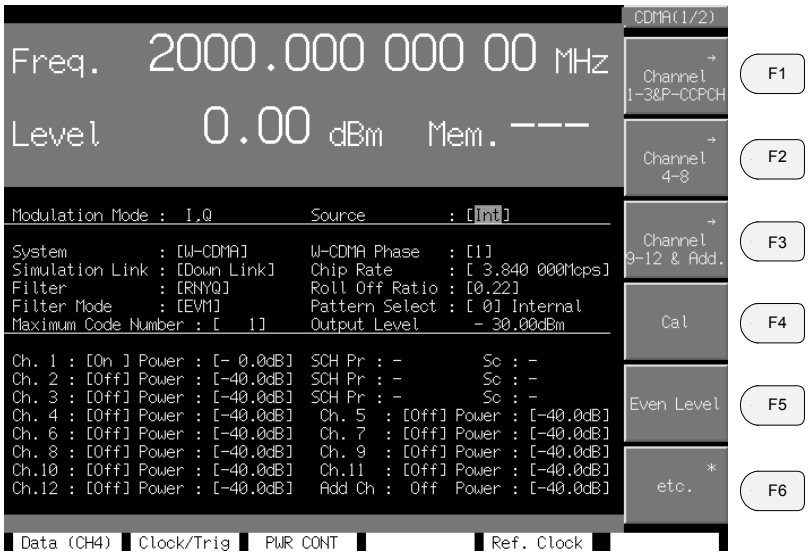
[3] Have the Spectrum Analyzer set to a 2 GHz center frequency and a 5 MHz frequency span to observe the Signal Generator output signal.

(2) Generate test signal

Image rejection and carrier leak adjustment involves vector modulation with a test signal in a sine waveform having a phase gap of $\pi/2$ rad between phases I and Q. Follow the steps below to perform vector modulation with a test signal.

[1] Press the modulation [Digital] key to turn on digital modulation.

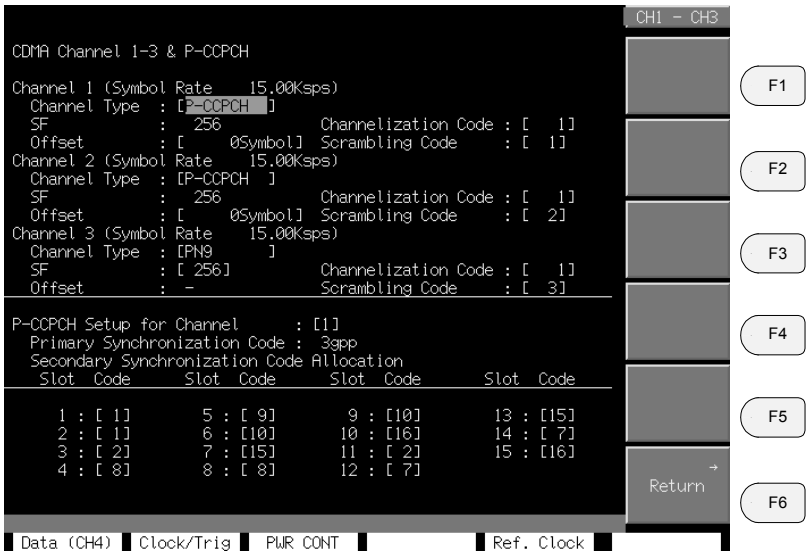
[2] Set Source to [Int] and System to [W-CDMA] on the digital modulation screen and perform digital modulation with the built-in MU368040A CDMA Modulation Unit.



[3] Set Filter Mode to [EVM].

[4] Using the MU368040A CDMA Modulation Unit, generate a test signal.

- Press [F1] (Channel 1-3) to display the CDMA Channel 1-3 screen.
- Set Channel 1 Channel Type to [16 bit Repeat] and Data to 1E1E.
- Set Channel 1 SF to [1].
- Set Channel 1 Scramble Code to [Off].

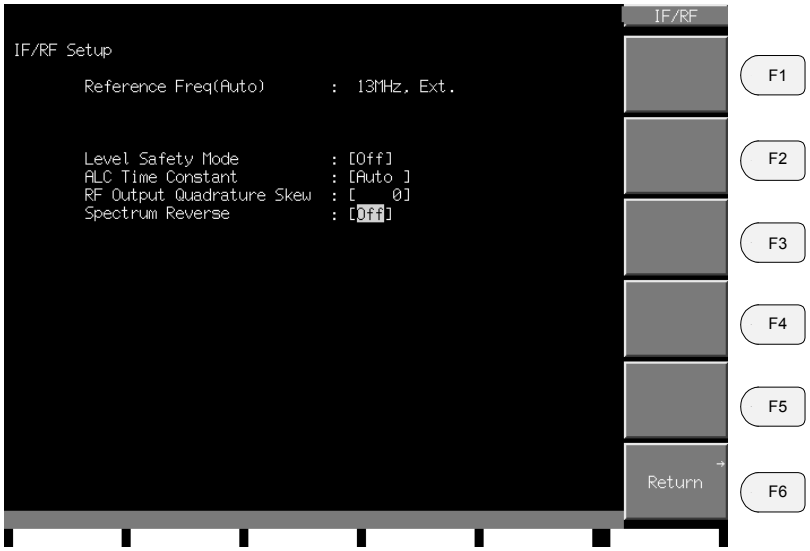


(3) Image rejection adjustment

[1] Warm-up for at least 1 hour at room temperature.

[2] Press [Config], [F1] (IF//RF Setup) in this sequence to display the IF/RF Setup screen.

[3] Using the cursor keys, move the reverse cursor to Spectrum Reverse.



[4] Toggle Spectrum Reverse between [On] and [Off] to adjust A2201 ASP R157 to get an equivalent image of the image signal level as observed on the Spectrum Analyzer.

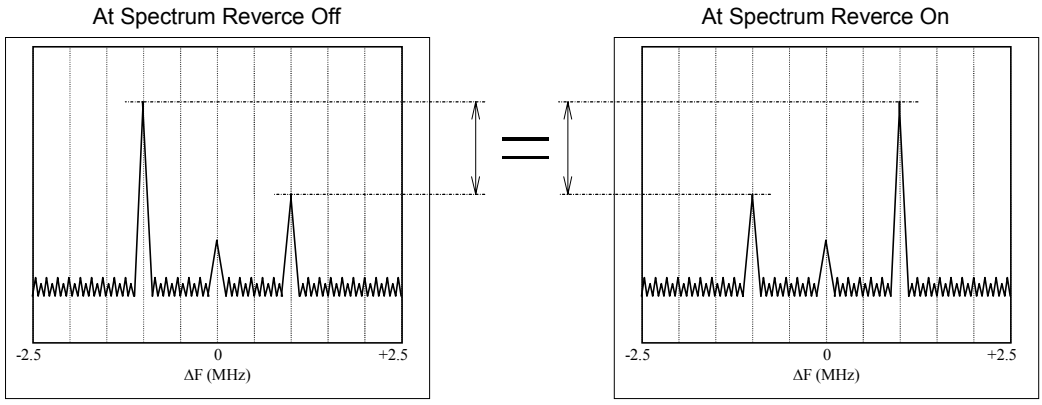


Fig.4-2 Image Signal Spectrum

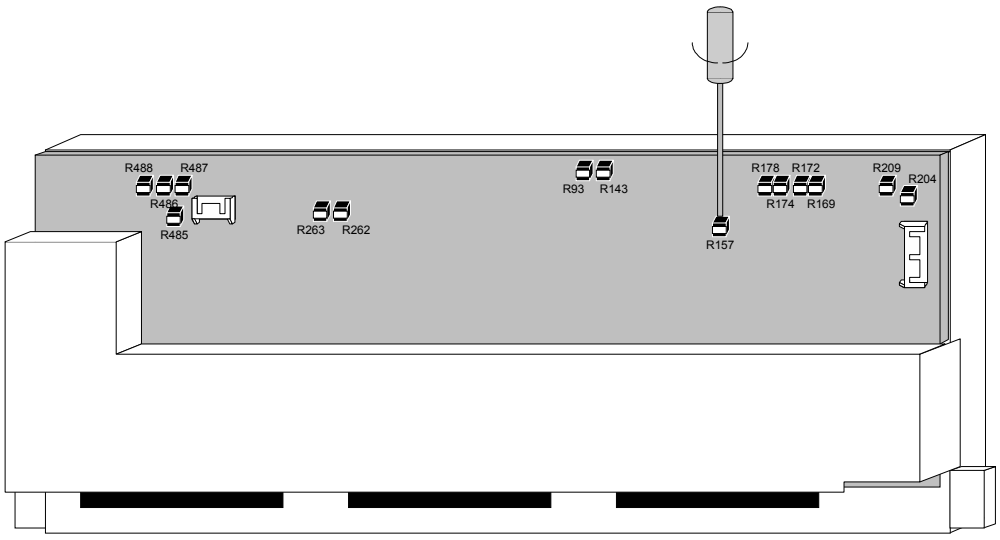


Fig.4-3 Image Signal Level Adjustment

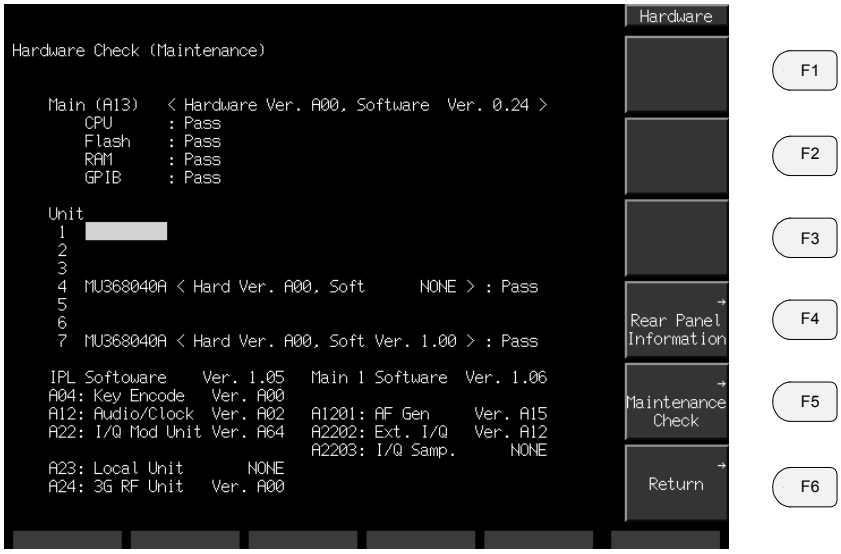
(4) Carrier Leak Adjustment

[1] Turn on the power while pressing the [Local] key. Continue pressing the [Local] key until the front-panel LED lights.

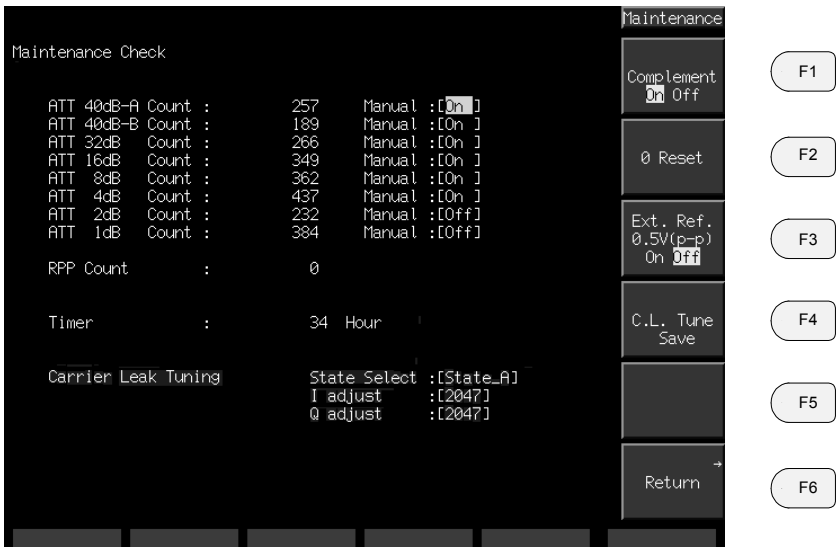
[2] When this equipment has started up, press [Config], [F1] (IF//RF Setup) in this sequence to display the IF/RF Setup screen.

[3] Press [Shift], [F5], [F1], [F2], [F3], [F4], [F5] in this sequence.

[4] Press [Config], [F5] (Hardware Check) in this sequence to display the Hardware Check (Maintenance) screen.



[5] Press [F5] (Maintenance Check) to display the Maintenance Check screen.



[6] Warm-up the MG3681A for at least 1 hour at room temperature with the top shield cover and top cover to be closed.

[7] Move the reverse cursor to "State Select" of Carrier Leak Tuning, using the cursor key.

[8] Set "State Select" to [State_A].

[9] Move the reverse cursor to "I adjust" and "Q adjust" of Carrier Leak Tuning, using the cursor key; to adjust the values of "I adjust" and "Q adjust" alternatively so that the carrier leak signal level becomes minimum.

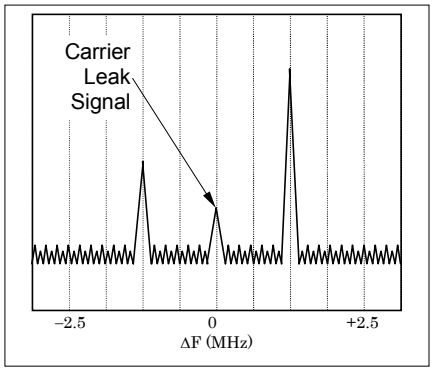


Fig.4-4 Carrier Leak signal spectrum

[10] After the adjustment completed, press [F4] (C.L. Tune Save) to write the adjustment data at EEPROM of A2201 ASP.

[11] Set the "State Select" to [State_B], [State_C], [State_D], [State_E], [State_F], [State_G] and [State_H], sequentially, to repeat the steps [9] and [10] above.

4.4 Output Level Compensation

Perform output level compensation on the MG3681A with regard to the three parameters: ALC linearity, frequency response, and step attenuator.

The output level will require recompensation when any of the following units has been replaced:

- A22 I/Q MOD UNIT
- A24 3G RF UNIT
- A26 POWER AMP UNIT
- Z2 S-ATT&RPP

(1) Installation

Set up a National Instruments PCI-GPIB or PCMCIA-GPIB card on a PC running Windows 95 or 98 and install driver software NI488.2.

Insert the install FD labeled "MG3681A Digital Modulation Signal Generator Compensation Software" into the floppy disk drive of the PC and run setup.exe. Proceed with installation by following instructions which appear on-screen. When the installation process is completed, the following files are stored in the destination folder:

- DMSG_CAL.exe — Executable file
- DMSG_CAL.ini — Configuration data backup file
- 3G_ATBL.tbl
- 3G_MTBL.tbl
- 3G_CTBL.tbl
- 3G_LTBL.tbl
- 6G_ATBL.tbl
- 6G_MTBL.tbl
- 6G_CTBL.tbl
- 6G_LTBL.tbl

  — Compensation frequency table files. These files must not be altered.

(2) Setup

As shown in Figure 4-5, connect the MG3681A that requires output level compensation, and the ML4803A power meter and the ML2530A calibration receiver for level measurement to the PC with a GPIB cable. Connect the MG3681A Buffer Output connector and the ML2530A Ext Reference connector with a coaxial cable with BNC connectors to synchronize their frequencies.

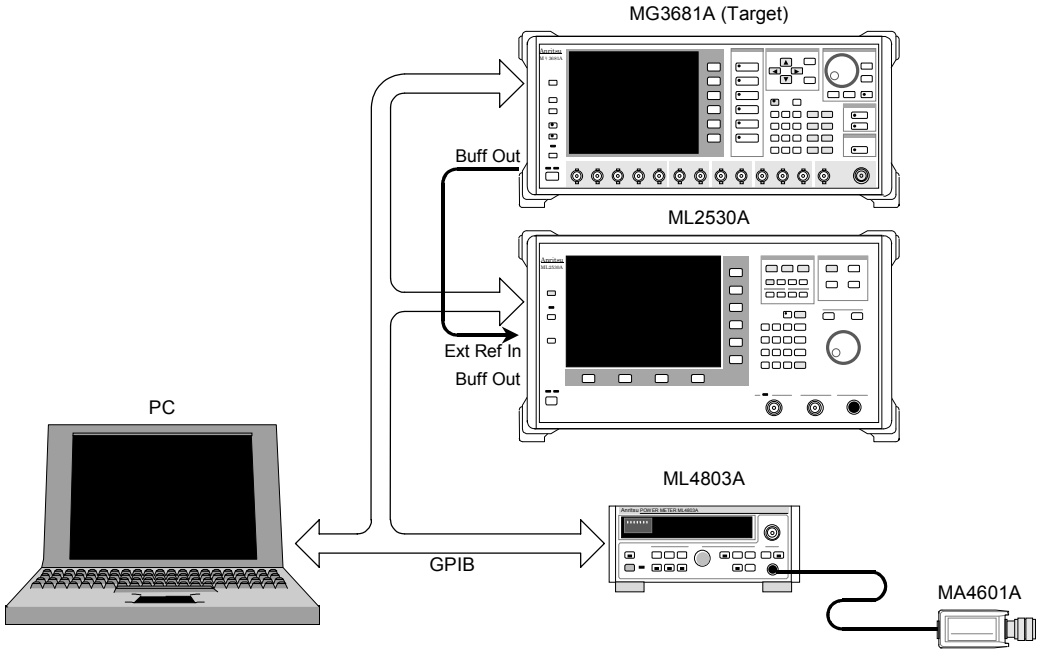


Fig.4-5 Setup

(3) Running compensation software

Run DMSG_CAL.exe to open the window shown in Figure 4-6.

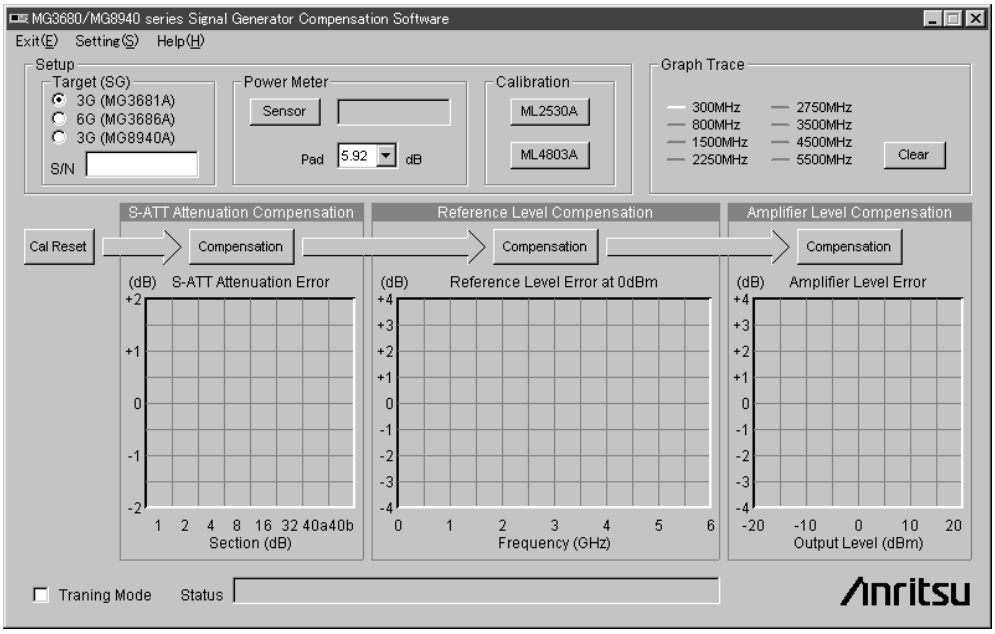


Fig.4-6 Compensation Software Window

(4) Creating a sensor calibration factor data file

Create the Cal. factor data file of the power sensor to be used for compensation, as follows.

Select the Sensor Cal. Factor on the Setting menu of the "MG3680 series Digital Modulation Signal Generator Compensation Software", to open the Power Sensor Cal Factor input window (Fig. 4-7).

Read the calibration values written on the MA4601A Power Sensor, then enter the parameters in the window.

After the entry completed, click [Save] to save the Cal. factor data file.

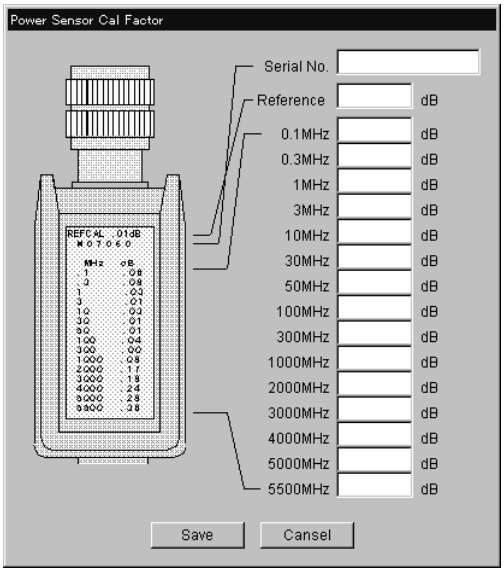


Fig.4-7 Sensor Calibration Data File Creation

(5) Configuration setting

MG3680 series Digital Modulation Signal Generator Compensation Software with regard to the following items:

[1] Target selection: Verify the target selection in the Setup section.
MG3681A: 3GHz

[2] Power sensor specification: Click [Sensor] in Power Meter in the Setup section to open the calibration factor data file that has been created in (1). Make sure that the serial number appears in the box to the right of the [Sensor] button.

[3] Pad attenuator setting: Enter a pad attenuation value for use in level measurement by the power meter at Pad value in Power Meter in the Setup section.

[4] GPIB address setting: Click [Interface Setup] on the setting menu to open a GPIB address setup window. Match the GPIB address of the MG3681A, ML2530A, and ML4803A.

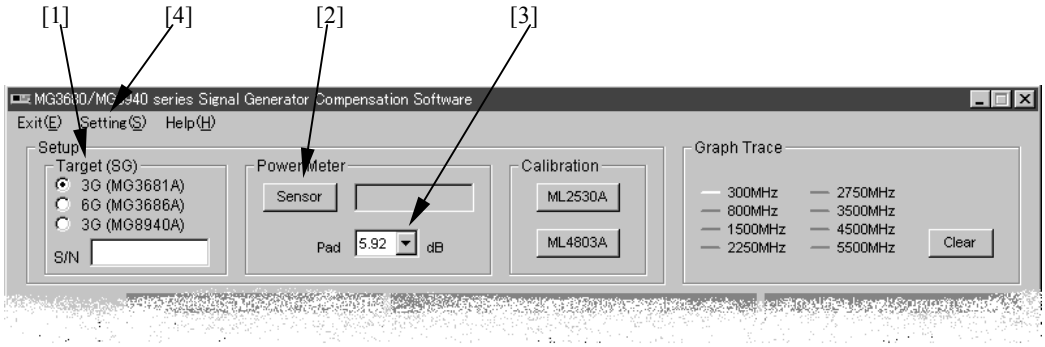


Fig.4-8 Compensation Software Configuration Setting

(6) Calibrating measuring instruments

Before proceeding with calibration, calibrate the ML4803A Power Meter and the ML2530A Calibration Receiver for level measurement. Have these instruments fully warmed-up at room temperature. Click [ML2530A] and [ML4803A] in Calibration in the Setup section and proceed with calibration by following instructions which appear on-screen.

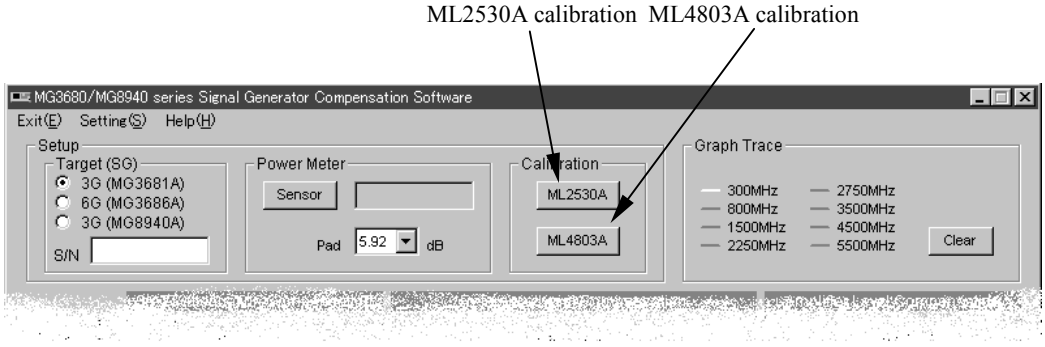


Fig.4-9 Calibrating Measuring Instruments

(7) Initializing compensation data

Initialize the level compensation data stored within the MG3681A.

Click [Cal Preset]. Initialization is completed when the message "Complete erase all compensation data" is displayed.

(8) Running S-ATT attenuation compensation

Compensate for the step attenuation of the MG3681A. Click [Compensation] in the S-ATT Attenuation Compensation section. Connect the MG3681A and the ML2530A with a cable as instructed on-screen. Select "Measure + Compensation" to run measurement, calculate compensation data and write the data.

(9) Running reference level compensation

Compensate for the frequency response of the MG3681A reference level.

Click [Compensation] in the Reference Level Compensation section. Connect the MG3681A, the ML2530A and the attenuator as instructed on-screen. Select "Measure + Compensation" to run measurement, calculate compensation data and write the data.

(10) Running amplifier level compensation

Compensate for the linearity of the MG3681A amplifier level.

Click [Compensation] in the Amplifier Level Compensation section. Connect the MG3681A, the ML2530A and the attenuator as instructed on-screen guidance. Select "Measure + Compensation" to run measurement, calculate compensation data and write the data.

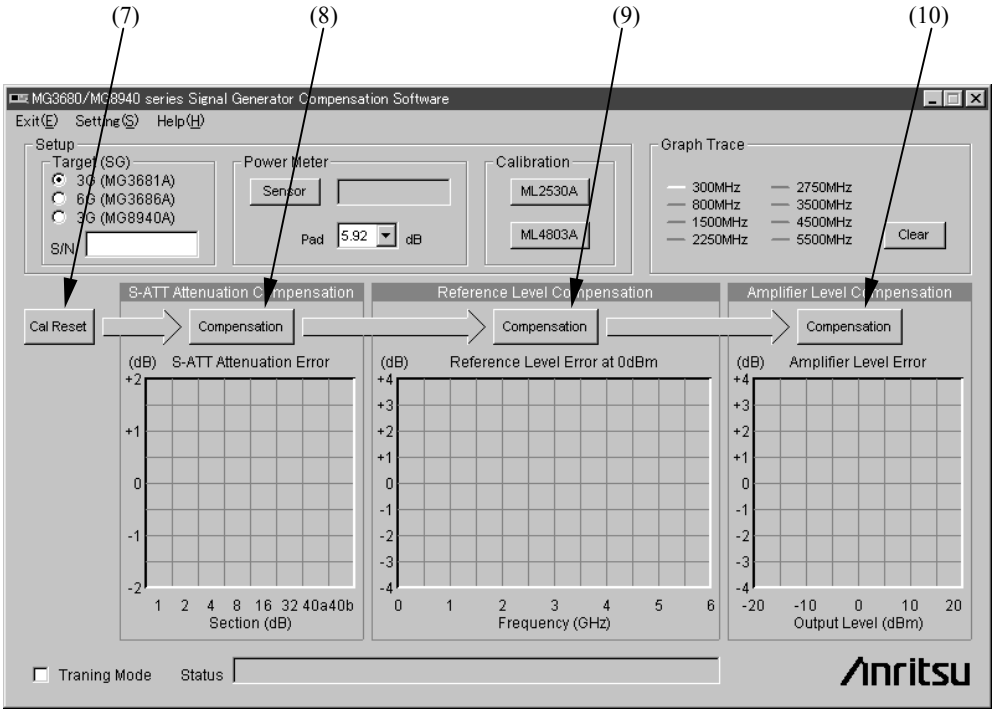


Fig.4-10 Running Compensation

4.5 Resetting S-ATT&RPP Counter

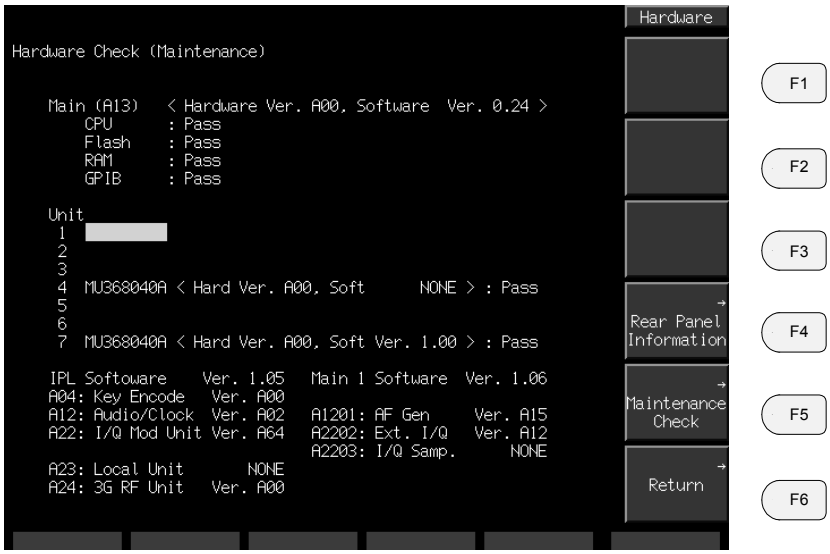
When the S-ATT&RPP in the MG3681A has been replaced, the operation counter must be reset. To reset the counter, follow these steps:

[1] Turn on the power while pressing the [Local] key. Continue pressing the [Local] key until the front-panel LED lights.

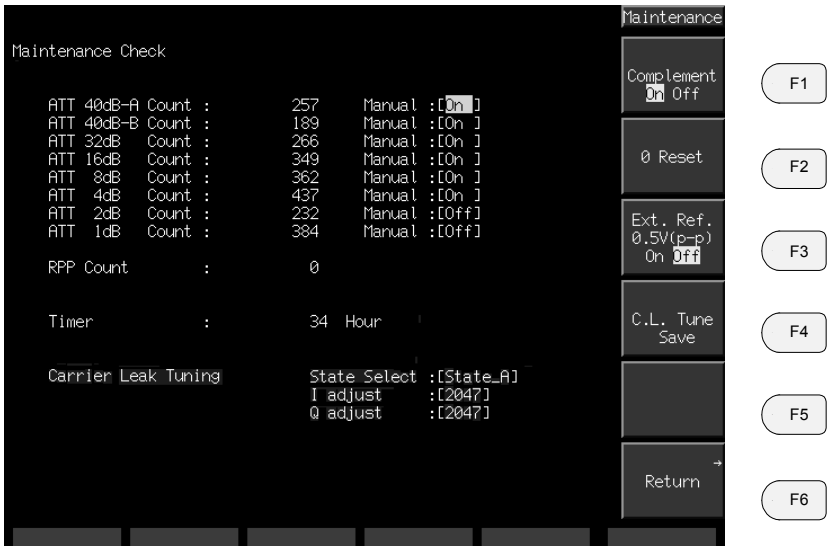
[2] When this equipment has started up, press [Config], [F1] (IF//RF Setup) in this sequence to display the IF/RF Setup screen.

[3] Press [Shift], [F5], [F1], [F2], [F3], [F4], [F5] in this sequence.

[4] Press [Config], [F5] (Hardware Check) in this sequence to display the Hardware Check (Maintenance) screen.



[5] Press [F5] (Maintenance Check) to display the Maintenance Check screen.



[6] Press [F2] (0 Reset) to initialize the S-ATT&RPP operation count at 0.

4-12.

SECTION 5
MECHANICAL CONFIGURATION

5.1 Outline

This section provides instructions on disassembling the MG3681A for repair.

Each numeral pointing to a unit or mechanical component in exploded views in Figures 5-1 to 5-9 is associated with a number in the parts lists in Tables 5-1 to 5-3.

CAUTION ⚠

Turn off the rear-panel power switch and disconnect the power cable from the receptacle before attempting to disassemble and reassemble this generator.

5.2 Cabinet and Shield Case Assembly

(1) Removing top cover [50]

Step	Procedure
1	Remove the four legs [80], [81], [84], and [85] from the top. (Figure 5-1).
2	Remove the screw securing top plate [50] from the rear. (Figure 5-1)
3	Remove top plate [50] by pulling it diagonally to the rear. (Figure 5-1)

(2) Removing top shield cover [41]

Step	Procedure
1	Remove all screws securing shielded case top cover [41]. (Figure 5-2)
2	Lift off the top cover [41]. (Figure 5-2)

(3) Removing bottom cover [51]

Step	Procedure
1	Remove sloped leg [86]. (Figure 5-1)
2	Remove the four legs [78], [79], [82], and [83] from the bottom. (Figure 5-1).
3	Remove the screw securing bottom plate [51] from the rear. (Figure 5-1)
4	Remove bottom plate [51] by pulling it diagonally to the rear. (Figure 5-1)

(4) Removing bottom shielding cover [42]

Step	Procedure
1	Remove all screws securing shielded case bottom cover [42]. (Figure 5-2)
2	Lift off the bottom cover [42]. (Figure 5-2)

(5) Removing front panel [70]

Step	Procedure
1	Remove exterior frame [75]. (Figure 5-1)
2	Remove the screws securing front plate [70] (four screws securing it to side frame [76] from the side and six securing it to front connector angle [48] from the bottom). (Figure 5-1)
3	Remove front plate [70] being careful not to cut the cable connection. (Figure 5-1)
4	Remove A1101 SWITCH BOARD [14] mounted on front plate [70] and cables W7, W8 and W9 connected to Display Assembly [15]. (Figure 5-7)

5.3 Main Unit Removal

5.3.1 Removing A03 REGULATOR [1]

Step	Procedure
1	Remove cables W1, W3, W4, and A01-W1 connected to A03 REGULATOR [1]. (Figure 5-4)
2	Remove five screws and four nuts securing A03 REGULATOR [1] to chassis [30]. (Figure 5-4)
3	Remove A03 REGULATOR [1]. (Figure 5-4)

5.3.2 Removing A04 KEY ENCODE [2]

Step	Procedure
1	Remove cables W7, W8, W9, W10, W13, and W14 connected to A04 KEY ENCODE [2]. (Figure 5-2)
2	Remove front connector angle [48]. (Figure 5-3)
3	Remove A04 KEY ENCODE [2]. (Figure 5-2)

5.3.3 Removing A05 REAR CONNECT [3]

Step	Procedure
1	Remove A05 REAR CONNECT [3] from shielded case rear plate [40], being careful not to cut the cable connection. (Figure 5-6)
2	Remove cable W12, A17 FAN ASSY [7], and A18 FAN ASSY [8] connected to A05 REAR CONNECT [3]. (Figure 5-4)

5.3.4 Removing A12 AUDIO/CLOCK [4]

Step	Procedure
1	Raise the ejector of A12 AUDIO/CLOCK [4] and pull it out from digital case [31]. (Figure 5-3)

5.3.5 Removing A13 MAIN CPU [5]

Step	Procedure
1	Raise the ejector of A13 MAIN CPU [5] and pull it out from digital case [31]. (Figure 5-3)

5.3.6 Removing A16 POWER SUPPLY UNIT [6]

Step	Procedure
1	Remove the radiation fin from A16 POWER SUPPLY UNIT [6]. (Figure 5-4)
2	Remove cables W1 and W2 connected to A16 POWER SUPPLY UNIT [6]. Take out W2 through the clearance and keep it towards the rear. (Figure 5-4)
3	Remove the screw securing A16 POWER SUPPLY UNIT [6] from the rear panel. (Figure 5-4)
4	Loosen the screw securing A16 POWER SUPPLY UNIT [6] to chassis [30]. (Figure 5-4)
5	Slide A16 POWER SUPPLY UNIT [6] to the front, then right and lift it off being careful to avoid the clamping screw head of chassis [30]. (Figure 5-4)

5.3.7 Removing A17 FAN ASSY [7]

Step	Procedure
1	Remove A05 REAR CONNECT [3] as instructed in Section 5.3.3.
2	Remove fan cover 2 [35] together with A17 FAN ASSY [7]. (Figure 5-6)
3	Remove A17 FAN ASSY [7] from fan cover 2 [35]. (Figure 5-6)

5.3.8 Removing A18 FAN ASSY [8]

Step	Procedure
1	Remove A05 REAR CONNECT [3] as instructed in Section 5.3.3.
2	Remove Fan Cover Assembly 1 [34] together with A18 FAN ASSY [8]. (Figure 5-6)
3	Remove A18 FAN ASSY [8] from Fan Cover Assembly 1 [34]. (Figure 5-6)

5.3.9 Removing A21 REFERENCE UNIT [9]

Step	Procedure
1	Remove reference rear plate [60] from shielded case rear plate [40] together with the angle and PC board. (Figure 5-5)
2	Remove A21 REFERENCE UNIT [9] by removing the two screws securing it to shielded case rear plate [40] and another two securing it to chassis [30]. (Figure 5-5)
3	Lift off A21 REFERENCE UNIT [9]. (Figure 5-5)

5.3.10 Removing A22 I/Q MOD UNIT [10]

Step	Procedure
1	Remove cables W11 and W21 connected to A22 I/Q MOD UNIT [10]. (Figure 5-3)
2	Remove the two screws securing A22 I/Q MOD UNIT [10] to chassis [30]. (Figure 5-3)
3	Lift off A22 I/Q MOD UNIT [10]. (Figure 5-3)

5.3.11 Removing A23 LOCAL UNIT [11]

Step	Procedure
1	Remove cable W22 connected to A23 LOCAL UNIT [11]. (Figure 5-3)
2	Remove the two screws securing A23 LOCAL UNIT [11] to chassis [30]. (Figure 5-3)
3	Lift off A23 LOCAL UNIT [11]. (Figure 5-3)

5.3.12 Removing A24 3G RF UNIT [12]

Step	Procedure
1	Remove cables W21, W22, and W25 connected to A24 3G RF UNIT [12]. (Figure 5-3)
2	Remove the two screws securing A24 3G RF UNIT [12] to chassis [30]. (Figure 5-3)
3	Lift off A24 3G RF UNIT [12]. (Figure 5-3)

5.3.13 Removing A1101 SWITCH BOARD [14]

Step	Procedure
1	Remove LCD bracket [74] from front plate [70]. (Figure 5-7)
2	Remove A1101 SWITCH BOARD [14] from front plate [70]. (Figure 5-7)

5.3.14 Removing A1102 DISPLAY ASSY [15]

Step	Procedure
1	Remove LCD bracket [74] from front plate [70]. (Figure 5-7)
2	Remove the backlighting cable of A1102 DISPLAY ASSY [15] from the backlighting inverter power supply connector [18]. (Figure 5-7)
3	Remove A1102 DISPLAY ASSY [15] from LCD bracket [74]. (Figure 5-7)

5.3.15 Removing Z2 S-ATT&RPP [16]

Step	Procedure
1	Remove cables W13, W25, and W29 connected to Z2 S-ATT&RPP [16]. (Figure 5-2)
2	Remove Z2 S-ATT&RPP [16] from shielded case front plate [39]. (Figure 5-2)

5.3.16 Removing U1 BACKLIGHTING INVERTER POWER SUPPLY [18]

Step	Procedure
1	Remove LCD bracket [74] from front plate [70]. (Figure 5-7)
2	Remove the backlighting cable of A1102 DISPLAY ASSY [15] from the connector of backlighting inverter power supply [18]. (Figure 5-7)
3	Remove inverter bracket [71] from LCD bracket [74]. (Figure 5-7)
4	Remove U1 BACKLIGHTING INVERTER POWER SUPPLY [18] from inverter bracket [71]. (Figure 5-7)

5.4 Built-in Option Unit

5.4.1 Built-in Opt 01/02 [20]/[21]

Step	Procedure
1	Remove reference rear plate [60] from shielded case rear plate [40] together with the angle and PC board. (Figure 5-5)
2	Remove A2103 STD OSC attached to the angle and attach A2104 STD OSC (Opt 01) [20] or A2105 STD OSC (Opt 02) [21] in its place. (Figure 5-5)
3	Attach reference rear plate [60] to the rear panel. (Figure 5-5)

5.4.2 Built-in Opt 11 [22]

Step	Procedure
1	Remove A22 I/Q MOD UNIT [10] as instructed in Section 5.3.10.
2	Replace the three screws securing A2201 ASP with poles. (Figure 5-8)
3	Attach A2202 EXT I/Q INTERFACE (Opt 11) [22]. (Figure 5-8)

5.4.3 Built-in Opt 21 [24]

Step	Procedure
1	Remove A12 AUDIO/CLOCK [4] as instructed in Section 5.3.4.
2	Attach six poles to A12 AUDIO/CLOCK [4]. (Figure 5-9)
3	Attach A1201 AF GENERATOR (Opt 21) [24]. (Figure 5-9)

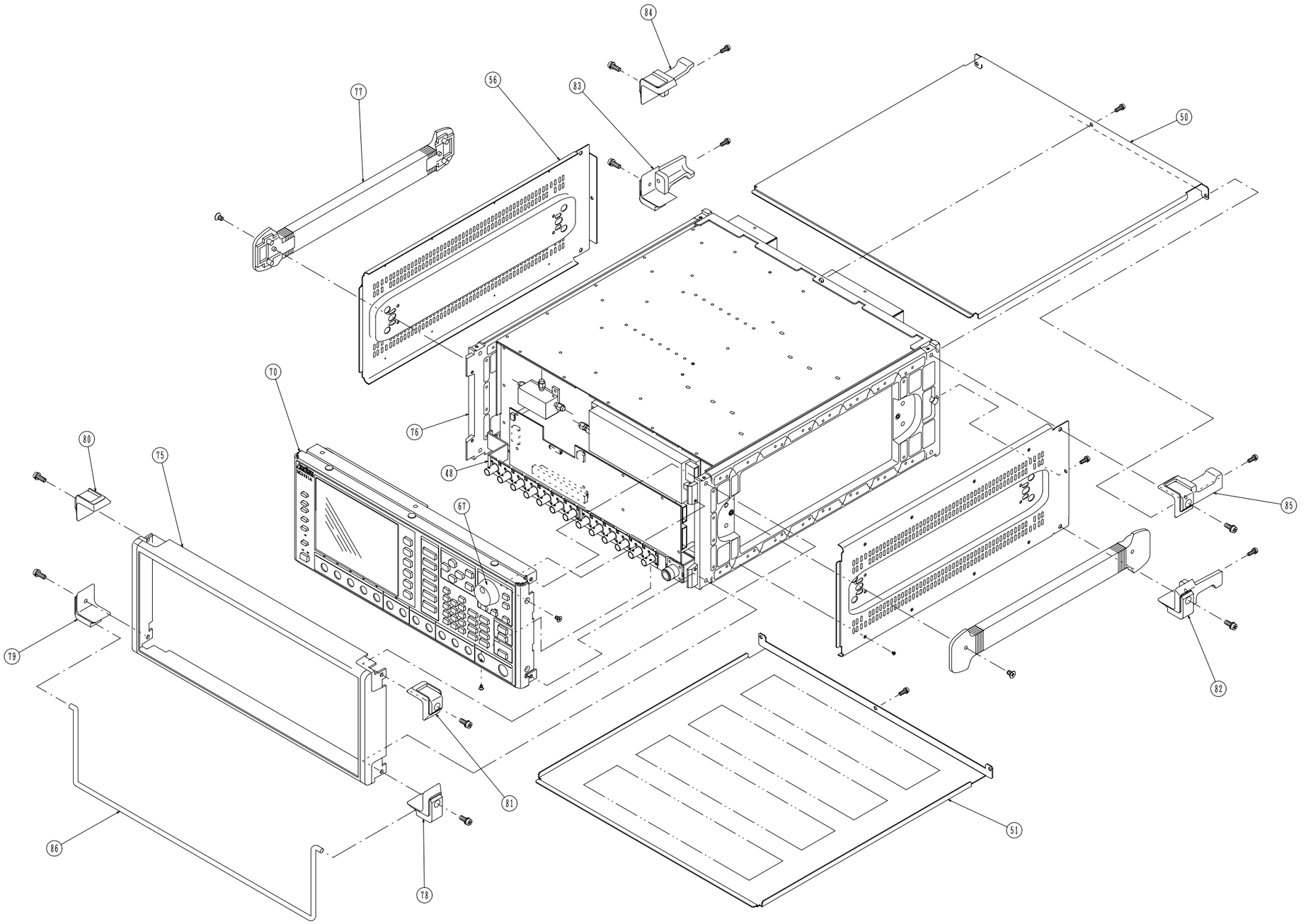


Fig.5-1

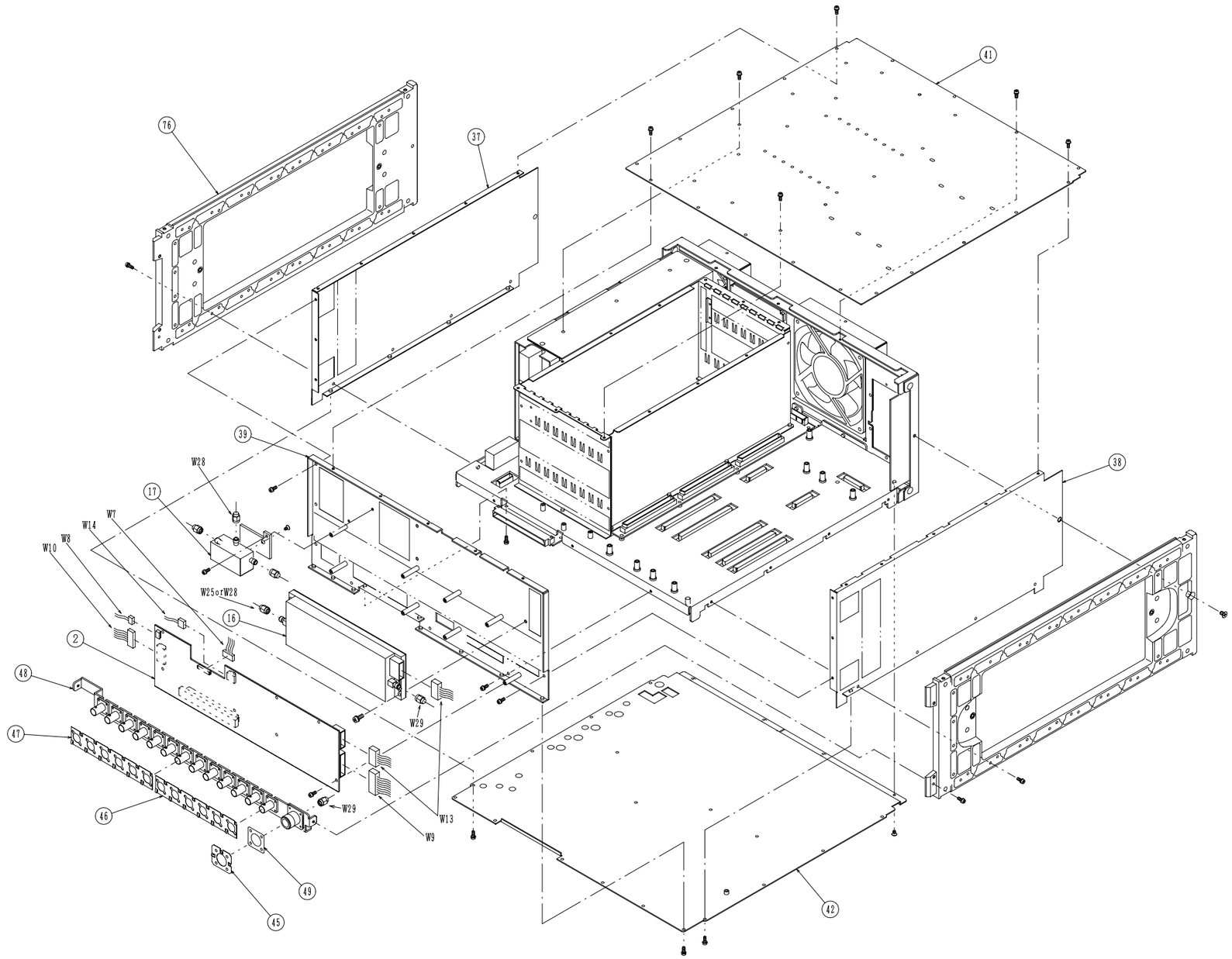

76
37
41
39
W28
17
W14
W7
W8
W10
W25or W28
16
2
48
47
46
49
45
W29
W29
W13
W9
38
42

Fig.5-2

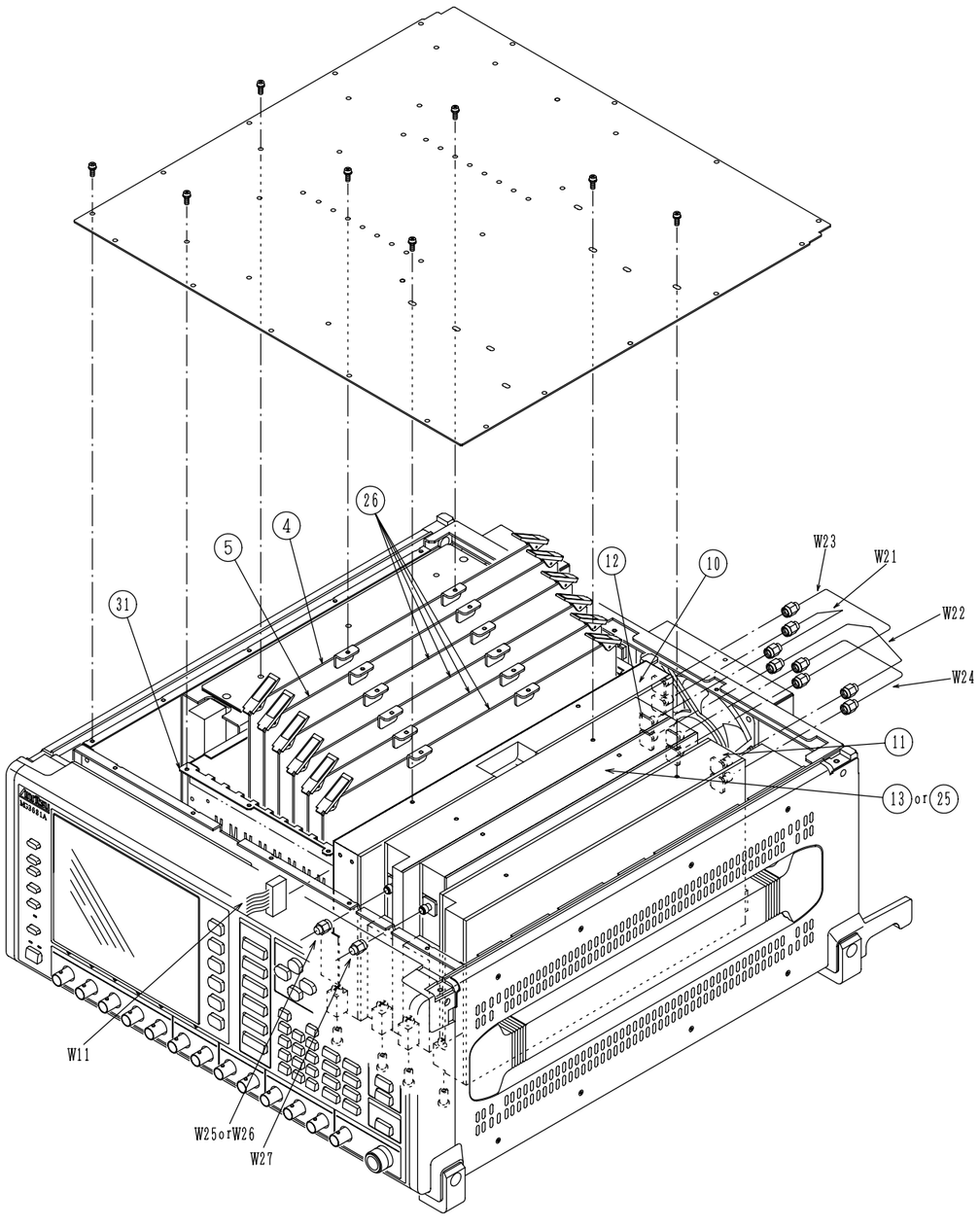


Fig.5-3

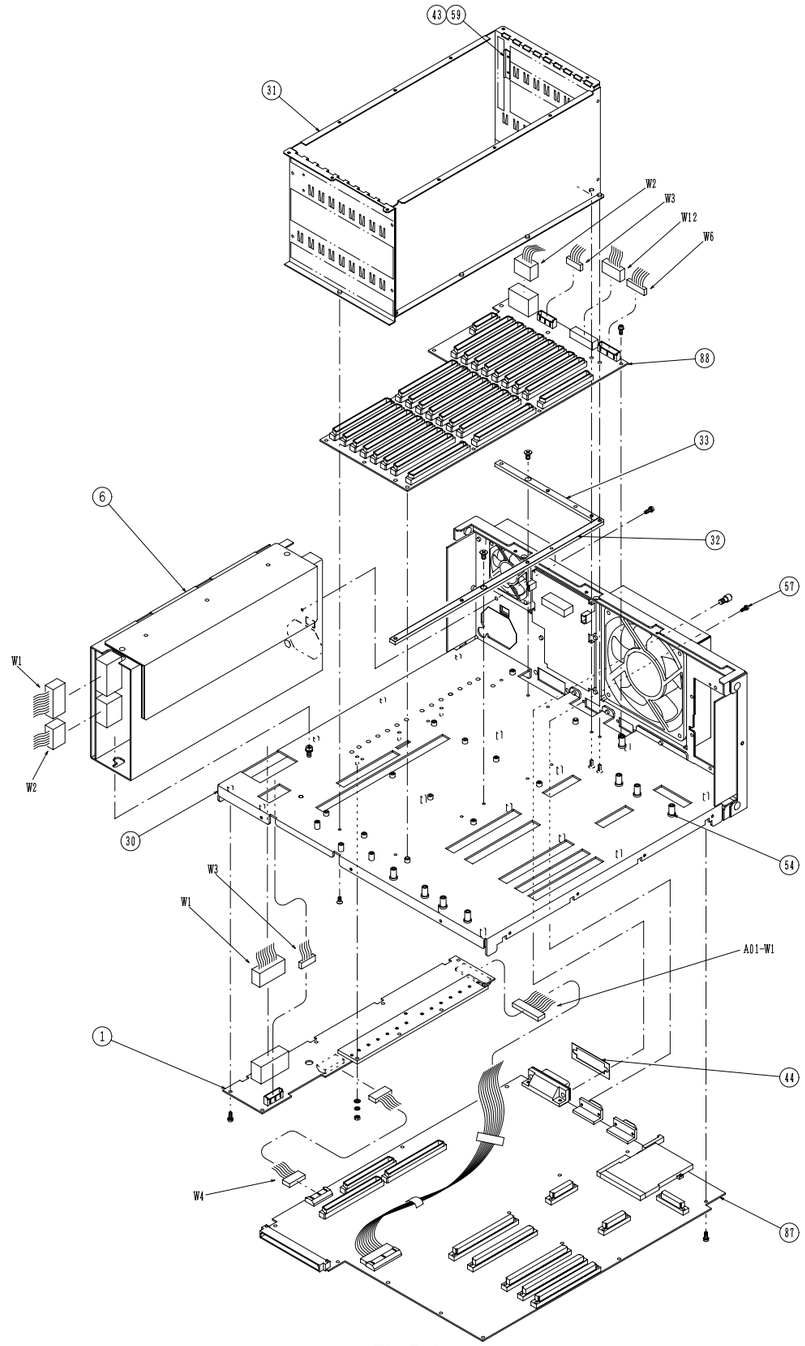


Fig.5-4

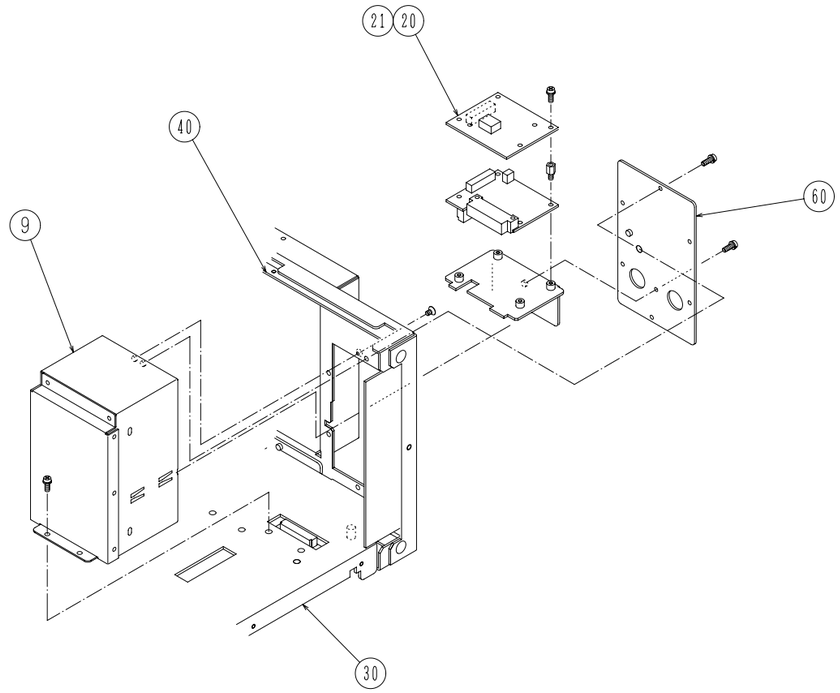


Fig.5-5

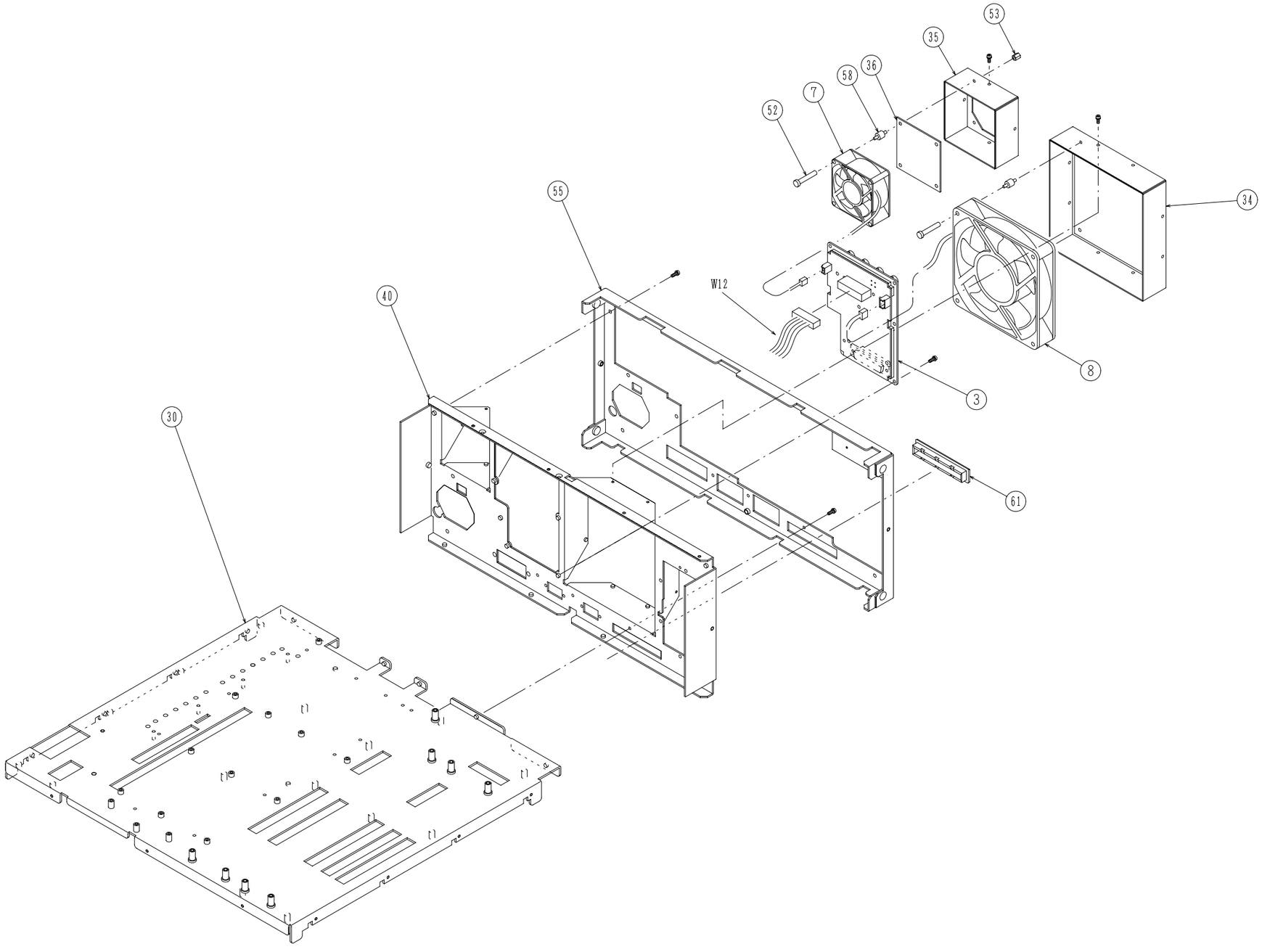


Fig.5-6

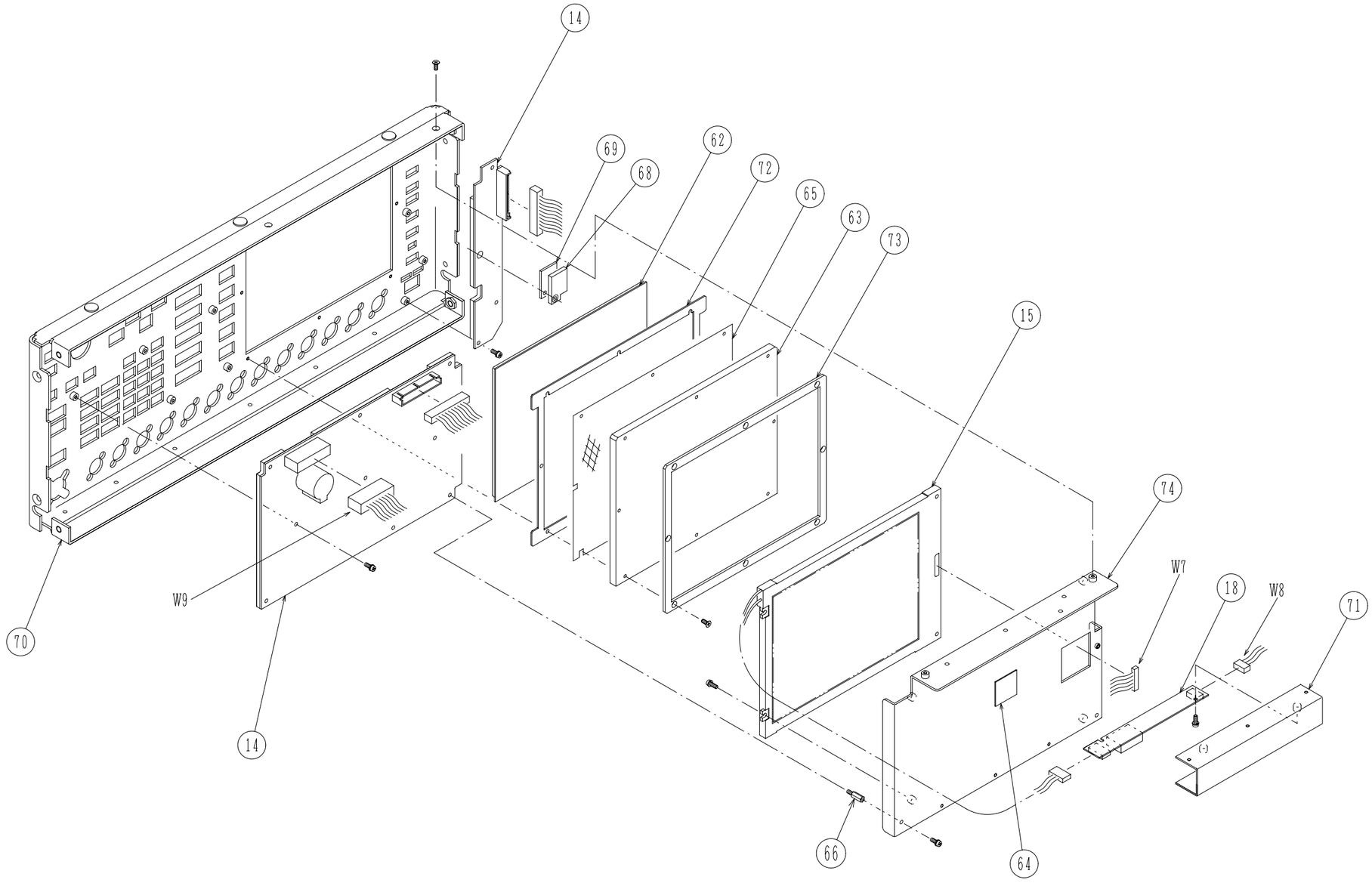


Fig.5-7

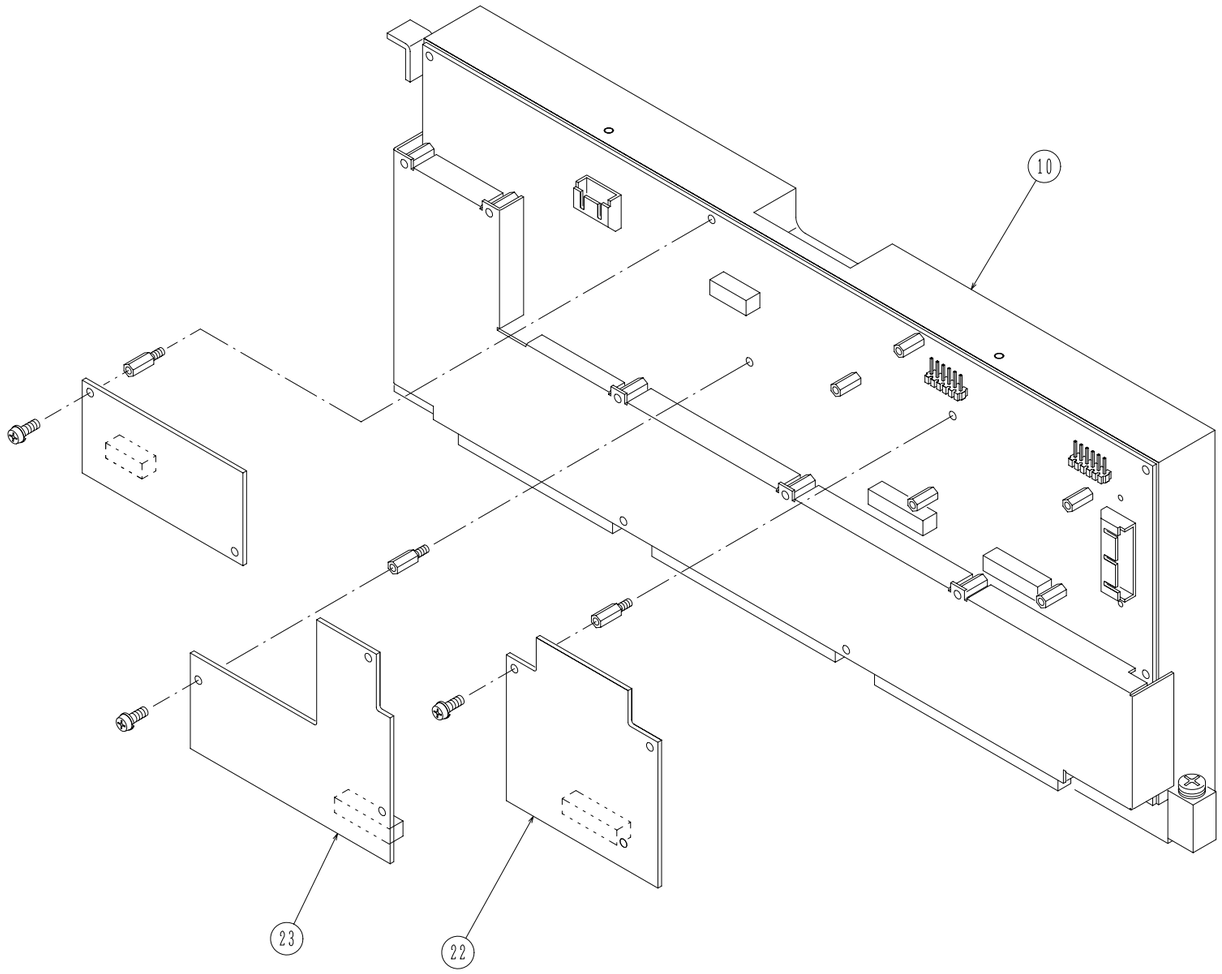


Fig.5-8

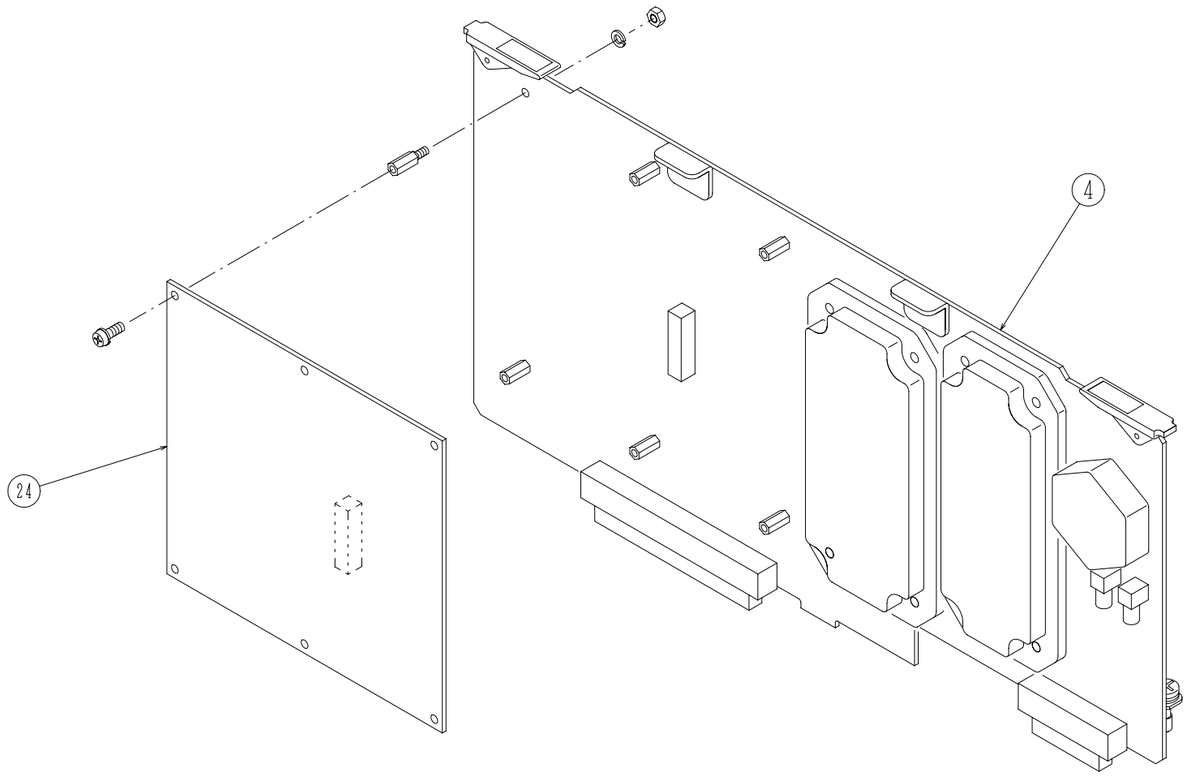


Fig.5-9

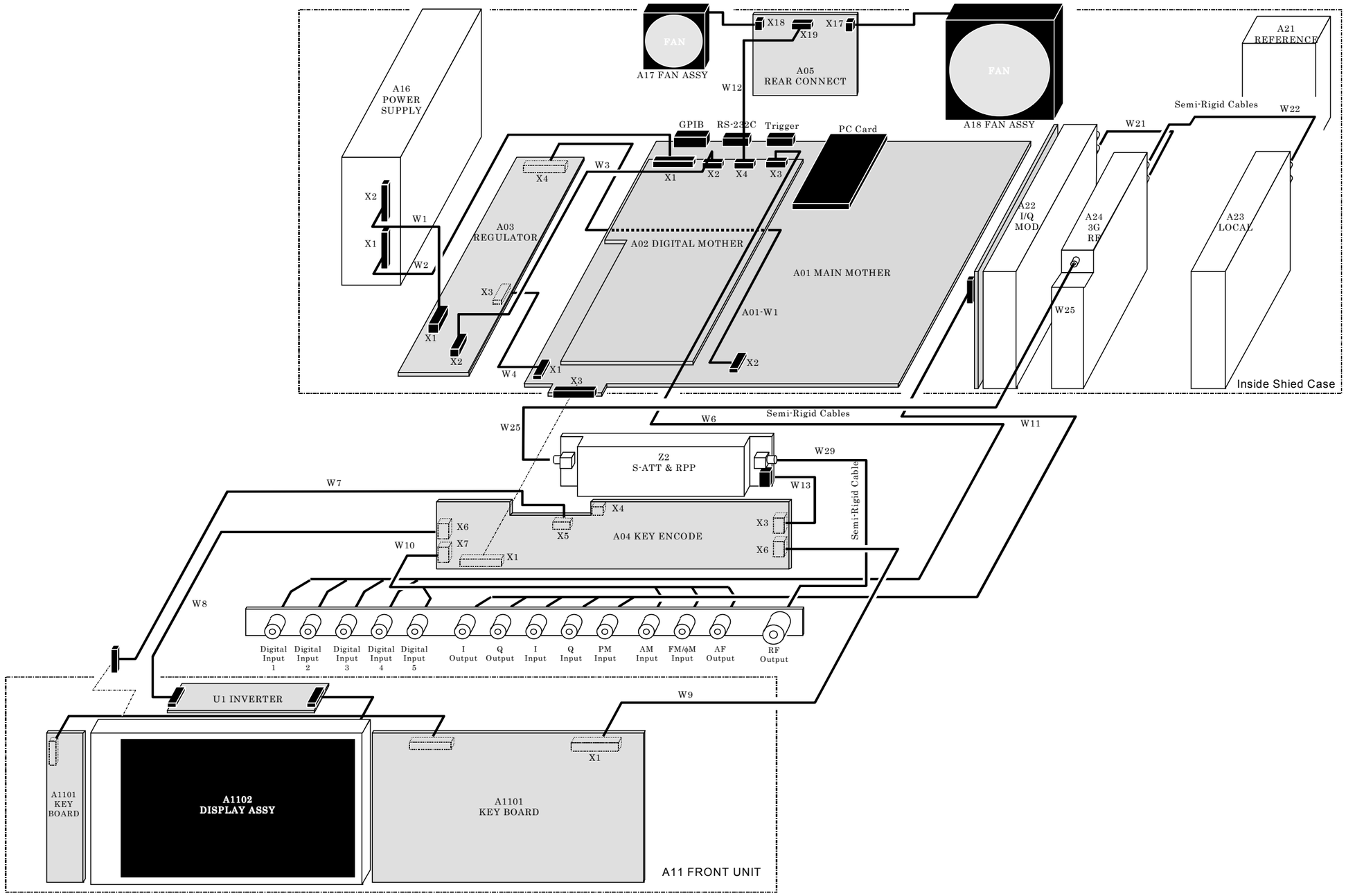


Fig.5-10 Cable Connection

5.5 Parts List

Table 5-1 Module List

No.	Order No.	Model No.	Name	Q'ty
1	34Y121692	MM300001A	A03 REGULATOR	1
2	34Y121693	MM300002A	A04 KEY ENCODE	1
3	34Y121694	MM300003A	A05 Rear CONNECT	1
4	34Y121542	MM300004A	A12 AUDIO/CLOCK	1
	34Y128895	MM300004B		
5	34Y124211	MM300005A	A13 MAIN CPU	1
6	34Y122055	MM300006A	A16 POWER SUPPLY UNIT	1
7	34Y124142	MM300007A	A17 FAN ASSY	1
8	34Y124141	MM300008A	A18 FAN ASSY	1
9	34Y124516	MM300010A	A21 REFERENCE UNIT	1
10	34Y124517	MM300011A	A22 I/Q MOD UNIT	1
	34Y124517C	MM300011B		
11	34Y124511	MM300012A	A23 LOCAL UNIT	1
12	34Y124519	MM300013A	A24 3G RF UNIT	1
14	34Y124416	MM300015A	A1101 SWITCH BOARD	1
15	34Y124751	MM300016A	A1102 DISPLAY ASSY	1
16	339H38476	339H38476	Z2 S-ATT&RPP	1
18	No.7235	PH-BLC08-K2	U1 BACKLIGHTING INVERTER POWER SUPPLY	1

Table 5-2 Option Parts List

No.	Order No.	Model No.	Name	Q'ty
20	34Y122396	MG3681A-01	REFERENCE CRYSTAL OSCILLATOR	1
21	34Y122397	MG3681A-02	REFERENCE CRYSTAL OSCILLATOR	1
22	34Y122370	MG3681A-11	ADDITIONAL FUNCTION OF I/Q OUTPUT	1
24	34Y122316	MG3681A-21	AF SYNTHESIZER	1
25	34Y129636	MG3681A-42	RF HIGH LEVEL OUTPUT	1

Table 5-3 Expansion Units List

No.	Order No.	Model No.	Name	Q'ty
26	34Y121955	MM300019A	A31 TDMA	1
	34Y122288	MM300017A	A32 CDMA	1
	34Y128899	MM300017B		
	34Y122649	MM300018A	A33 DIGITAL FILTER	1
	34Y128901	MM300018B		
	34Y129057	MM300022A	A37 C/N CONT	1
	34Y126190	MM300024A	A38 20Msps ARB	1

Table 5-4 Mechanical Parts List

No.	Parts No.	Name	Remarks	Q'ty
30	322B14661	Chassis		1
31	333B43579	Digital Case Assembly		1
32	33B43870	Spacer 1 for Digital Case		1
33	34B124061	Spacer 2 for Digital Case		1
34	342B124938	Fan Cover Assembly 1		1
35	34B124937	Fan Cover 2		1
36	34B102813Q	Guard		1
37	332B43581	Shield Case, Left Side		1
38	332B43582	Shield Case, Right Side		1
39	332B43583	Shield Case, Front		1
40	322B14666	Shield Case, Rear		1
41	32B14696	Shield Case Cover, Top		1
42	322B14697	Shield Case Cover, Bottom		1
43	34B99044	Guide Bracket		2
44	34B97090	Plate		1
45	34B122802	N Connector Spring		1
46	33B43718F	BNC Connector Spring		1
47	33B43718G	BNC Connector Spring		1
48	33B43558	Bracket for Front Connector		1
49	34B122350	Spacer for N Connector		1
50	33B32676	Special Cover, Top	1MW450D	1
51	33B43727	Special Cover, Bottom	1MW450D	1
52	44H87316E	Fan Nut		8
53	44H87315	Nut		8
54	34H97218	Guide Pin		8
55	323B14692	Rear Panel		1
56	332B44441	Special Cover, Side	4U450D	2
57	No.1305	RDG-LNA(4-40)		4
58	No.1062	ME-7 CR50		8
59	34B99043	Spring		2
60	343B122824	Rear Panel for REFERENCE		1
61	33E43559	PMC Bezel		1
62	33E43983	Filter1		1
63	33E43986B	Filter2		1
64	S4N21943	High Voltage Label		1
65	34B122337	Shielding Mesh		1
66	Z4H300061	Support		2
67	33E32858	Knob, Encoder		1
68	34B125048	Spacer for LCD		1
69	34B125049	Spacer for LCD2		1
70	322B14659	Front Panel		1
71	342B122336	Bracket for Inverter		1
72	33B43981	Plate1 for Filter		1
73	33B43982	Plate2 for Filter		1
74	332B43553	Bracket for LCD		1
75	32E11762	Bezal, Front	1MW4U	1
76	332B44398	Side Frame	4U450D	2
77	339E32669	Handle	450D	2
78	32E11801	Foot, Front Right Side Bottom		1
79	32E11801B	Foot, Front Left Side Bottom		1
80	32E11802	Foot, Front Left Side Top		1
81	32E11802B	Foot, Front Right Side Top		1
82	32E11803	Foot, Rear Right Side Bottom		1
83	32E11803B	Foot, Rear Left Side Bottom		1
84	32E11804	Foot, Rear Left Side Top		1
85	32E11804B	Foot, Rear Right Side Top		1

No.	Parts No.	Name	Remarks	Q'ty
86	34B101778	Tilt Stand	1MW	1
87	34Y121690	A01 MAIN MOTHER		1
88	34Y121691	A02 DIGITAL MOTHER		1

5-20.